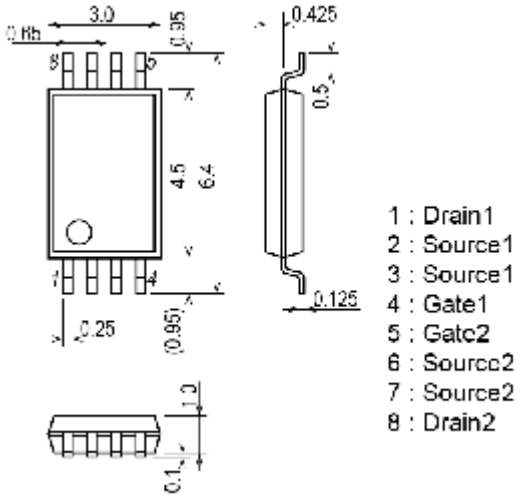
Dual N-Channel Enhancement Mode MOSFET

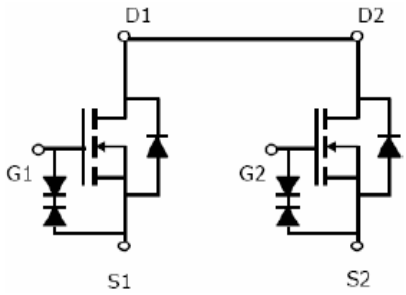
DESCRIPTION

The UC1870 uses advanced trench technology to provide excellent RDS(ON),low gate charge. These device are particularly suited for use as a load switch or in PWM application. It is ESD protected.



GENERAL FEATURES

- V_{DS}=20V,I_D=7A
  $R_{DS(ON)}$=16mΩ(typ)@V_{GS}=4.5V
  $R_{DS(ON)}$=20mΩ(typ)@V_{GS}=2.5V
  $R_{DS(ON)}$=28mΩ(typ)@V_{GS}=1.8V
- Low ON-resistance
- Lead free product is acquired
- Surface Mount Package
- ESD Rating:2000V HBM



Application

- Battery protection
- Load switch
- Potable Equipment

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
A1870	UC1870	TSSOP8	330mm	12mm	3000

Absolute Maximum Ratings (T_A=25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	7	A
Drain Current-Continuous @Current-Pulsed(Note 1)	I_{DM}	30	A
Maximum Power Dissipations (25℃)	P_D	1.48	W
Maximum Junction Temperature	T_J	150	℃

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient(Note2)	$R_{\theta JA}$	83.3	℃/W

Electrical Characteristics (T_A=25°C Unless Otherwise Noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=18V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V, V_{DS}=0V		±3	±10	uA
ON CHARACTERISTICS(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.55	0.7	1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=6A		16	19	mΩ
		V_{GS}=2.5V, I_D=5.2A		20	24	
		V_{GS}=1.8V, I_D=5A		28	32	
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=4.5A	4.5			S

Electrical Characteristics (Cont.)(T_A=25°C Unless Otherwise Noted)

DYNAMIC CHARACTERISTICS(Note 4)						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,F=1.0MHZ		1300		PF
Output Capacitance	C_{oss}			190		PF
Reverse Transfer Capacitance	C_{rss}			154		PF
SWITCHING CHARACTERISTICS(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V,V_{GS}=4.5V,R_{GEN}=3Ω,Rl=1.35Ω		7		ns
Turn-on Rise Time	t_r			15		ns
Turn-off Delay Time	$t_{d(off)}$			53		ns
Turn-off Fall Time	t_f			17		ns
Total Gate Charge	Q_g	V_{DS}=10V,I_D=6A,V_{GS}=4.5V		23		nc
Gate-Source Charge	Q_{gs}			2		nc
Gate-Drain Charge	Q_{gd}			3.4		nc
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage(Note 3)	V_{SD}	V_{GS}=0V,I_S=1.7A		0.8	1.3	V
Diode Forward Current(Note 2)	Is				7	A

NOTES:

1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.Surface Mounted on FR4 Board, t≤10 sec.

3.Pulse Test: Pulse Width≤300uS,Duty Cycle≤2%

4.Guaranteed by design, not subject to production testing.

Typical Characteristics

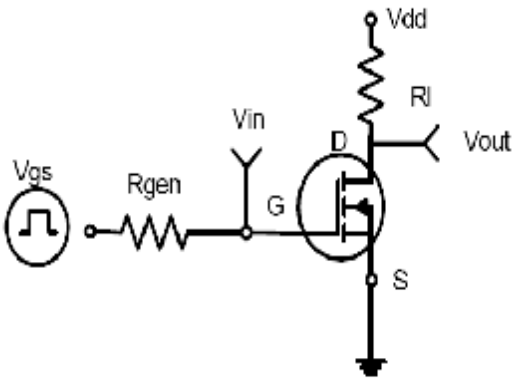


Figure 1:Switching Tset Circuit

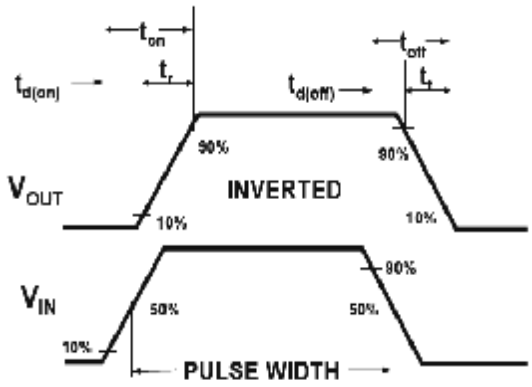


Figure 2:Switching Waveforms

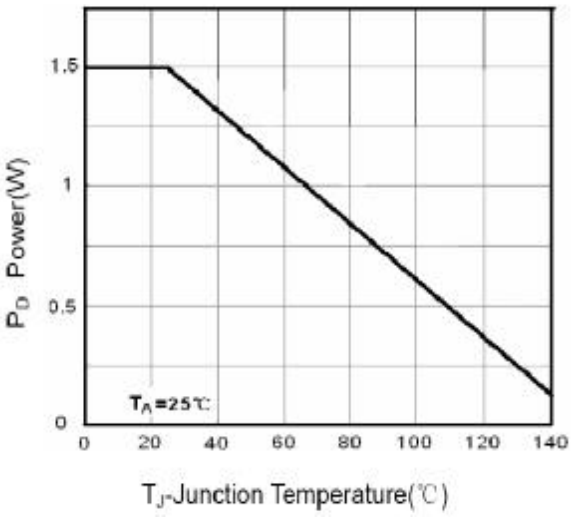


Figure 3:Power Dissipation

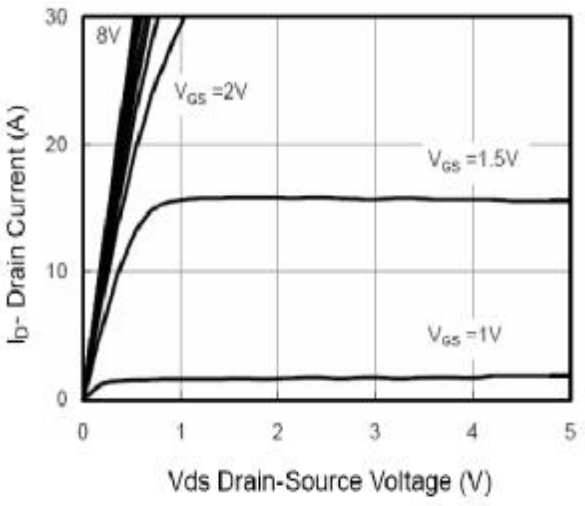


Figure 4:Output Characteristics

Typical Characteristics

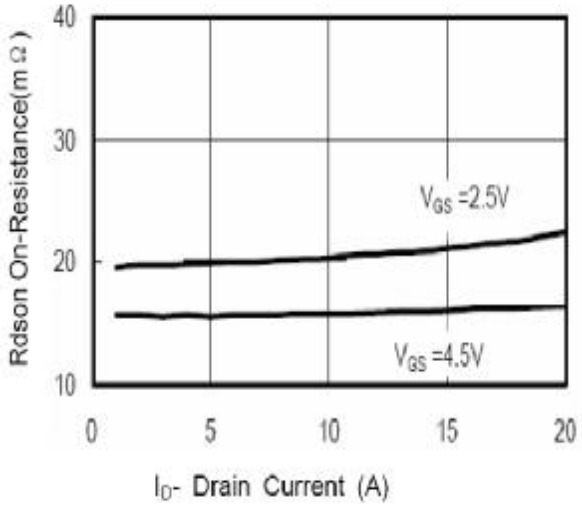


Figure 5:Drain-Source On-Resistance

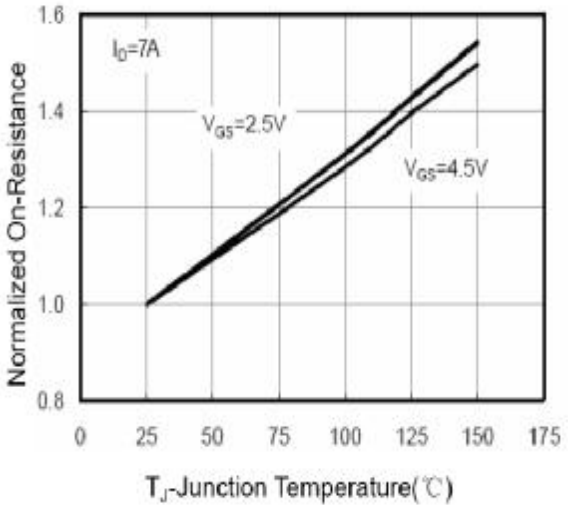


Figure 6:Drain-Source On-Resistance

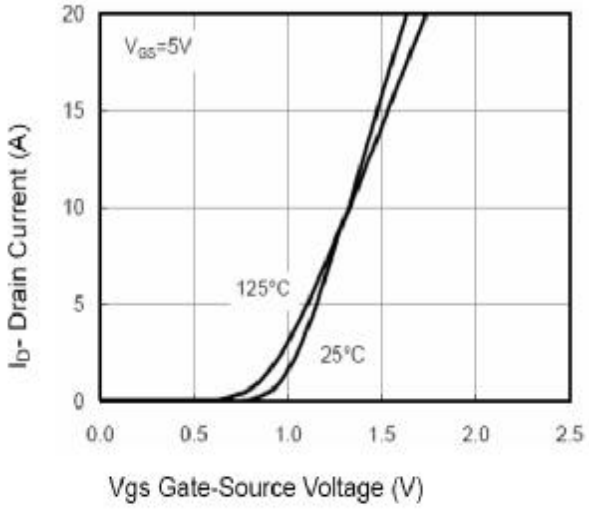


Figure 7:Transfer Characteristics

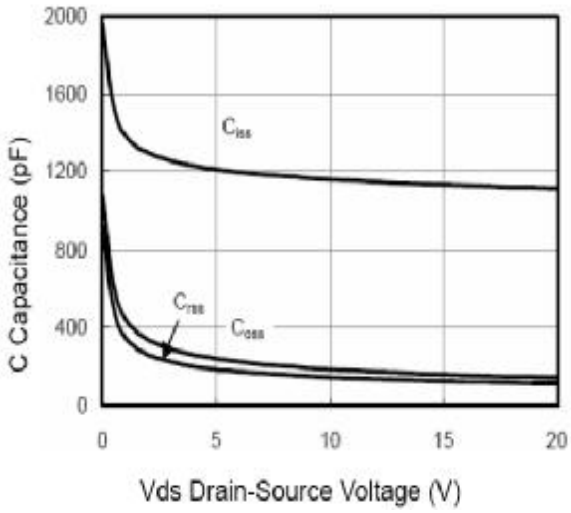


Figure 8:Capacitance vs Vds

Typical Characteristics

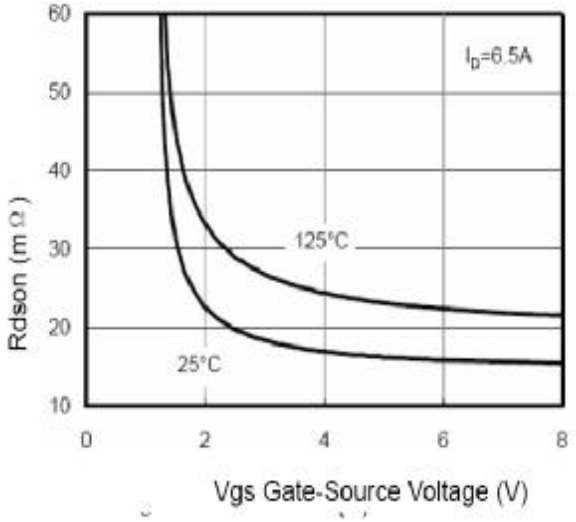


Figure 9:Rdson vs Vgs

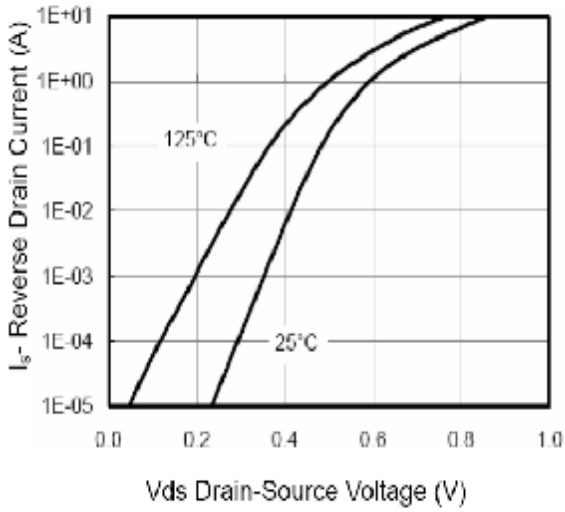


Figure 10:Reverse Drain Current VS Vds

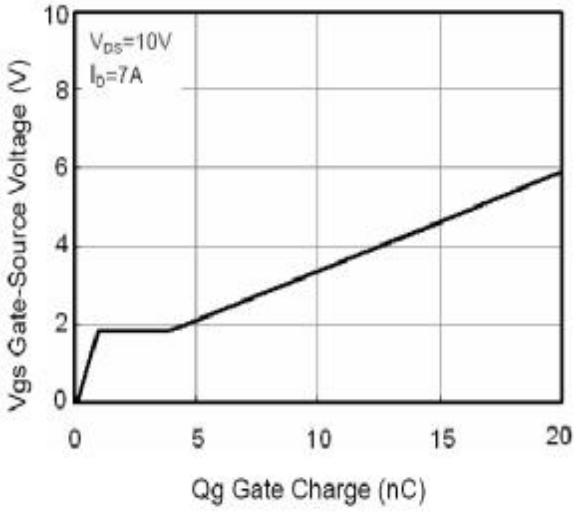


Figure 11:Gate Charge

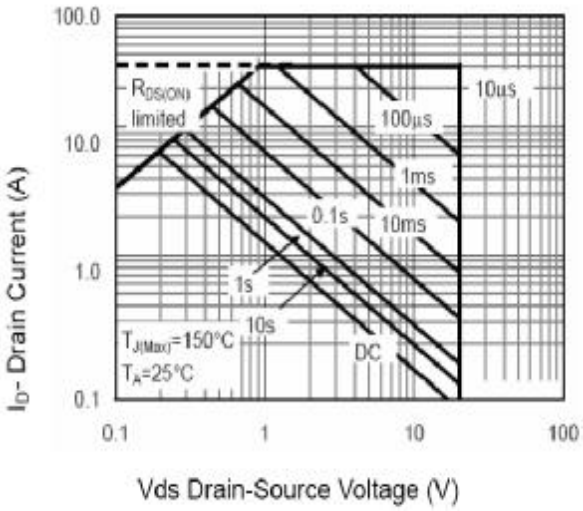


Figure 12:Safe Operation Area

Typical Characteristics

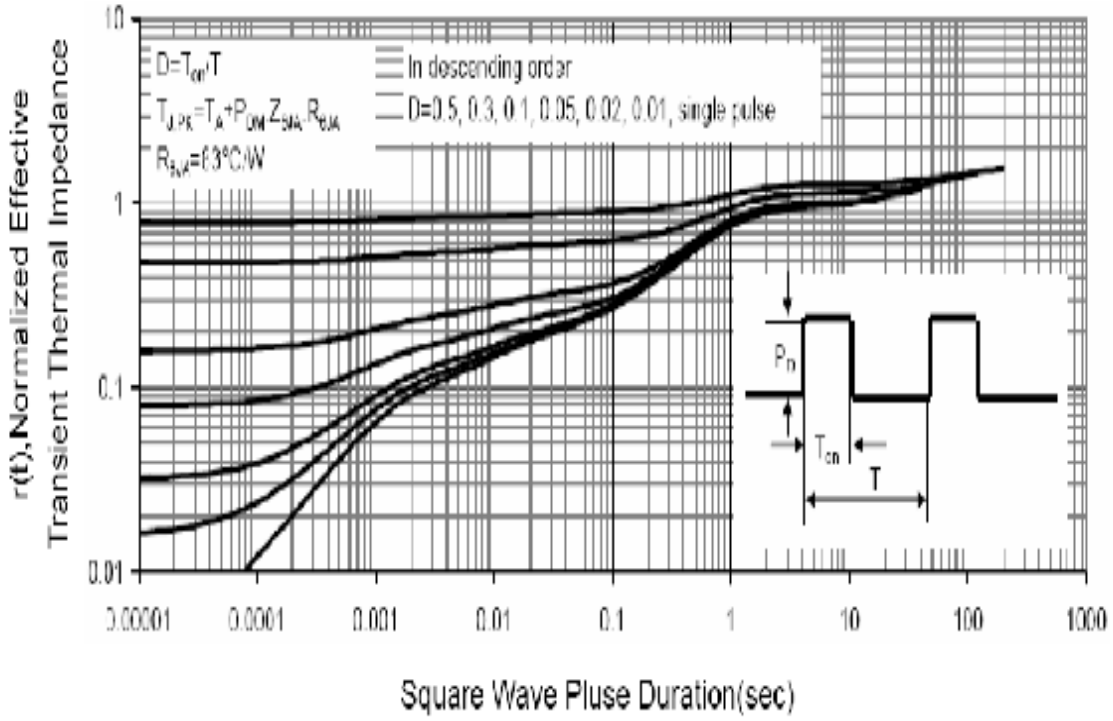
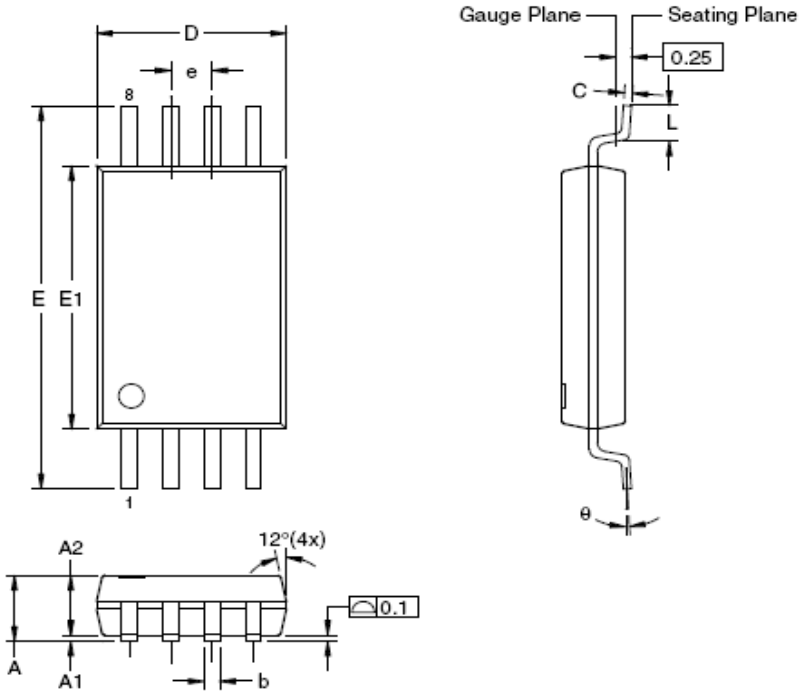
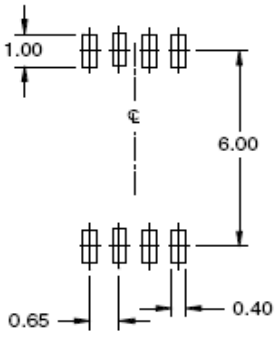


Figure 13:Normalized Maximum Transient Thermal Impedance

Package Information



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

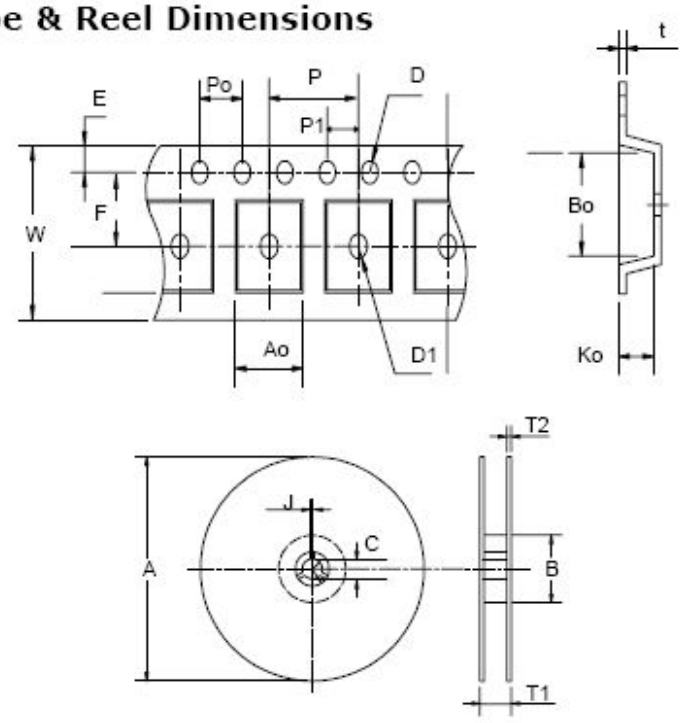
Dimensions in inches

Symbols	Min.	Nom.	Max.
A	—	—	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
b	0.007	—	0.012
C	0.004	—	0.008
D	0.114	0.118	0.122
E	0.252 BSC		
E1	0.169	0.173	0.177
e	0.026 BSC		
L	0.018	0.024	0.030
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
6. Refer to JEDEC MO-153(AA).

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
TSSOP-8	330 ± 1	62 +1.5	12.75+0.15	2 + 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0. 1	1.5 + 0.1	1.5 + 0.1	4.0 ± 0.1	2.0 ± 0.1	7.0 ± 0.1	3.6 ± 0.3	1.6 ± 0.1	0.3±0.013

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C,5 SEC
HOLT	MIL-STD 883D-1005.7	1000 Hrs Bias @ 125°C
PCT	JESD-22-B, A102	168 Hrs, 100% RH, 121°C
TST	MIL-STD 883D-1011.9	-65°C ~ 150°C, 200 Cycles

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