Genesys Logic, Inc.

GL823

USB 2.0 SD/MMC Card Reader Controller

Datasheet

Revision 1.08
Dec. 11, 2014

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Genesys Logic, Inc.
12F., No. 205, Sec. 3, Beixin Rd., Xindian Dist. 231,
New Taipei City, Taiwan
Tel : (886-2) 8913-1888
Fax : (886-2) 6629-6168
http ://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	09/18/2009	First formal release
1.01	12/15/2009	Add QFN 24 package
1.02	03/11/2010	Remove USB DP/DM port swap feature, p.7 & p.11 Modify Ch6 Package Dimension, p.19 Modify Ch7 Ordering Information, p.21
1.03	06/28/2010	Add Table 2.1: Product Difference Overview, p.7
1.04	03/07/2013	Modify Ch5.1 and Ch5.2, p.15
1.05	04/17/2013	Add GL823-OGY in Ch7, p21
1.06	04/24/2013	Add Note1in Ch2, p7
1.07	02/25/2014	Modify Ch6 Package Dimension, p.20
1.08	12/11/2014	Add T_j in Ch5.3, p.16

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CHAPTER 1 GENERAL DESCRIPTION

The GL823 is a USB 2.0 SD/MMC Flash Card Reader single chip. It supports USB 2.0 high-speed transmission to Secure Digital™ (SD), SDHC, SDXC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro, MMCmobile on one chip. As a single chip solution for USB 2.0 flash card reader, the GL823 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and SD/MMC card interface specification.

The GL823 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and flash card interfaces. Its' pin assignment design fits to card sockets to provide easier PCB layout. Inside the chip, it integrates 5V to 3.3V and 3.3V to 1.8V regulators and power MOSFETs and it enables the function of on-chip clock source (OCCS) which means no external 12MHz XTAL is needed and that effectively reduces the total BOM cost.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0
  - Comply with USB Storage Class specification rev. 1.0
  - Support one device address and up to four endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3)
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 12 clocks per instruction cycle
  - Embedded mask ROM and internal SRAM
- Secure Digital™ (SD) and MultiMediaCard™ (MMC) *Note1
  - Support SD specification v1.0 / v1.1 / v2.0/ SDHC (Up to 32GB)
  - Compatible with SDXC (Up to 2TB)
  - Support MMC specification v3.x / v4.0 / v4.1 / v4.2.
  - x1 / x4 bit data bus
- On chip clock source and no need of 12MHz Crystal Clock input.
- On-Chip 5V to 3.3V and 3.3V to 1.8V regulators
- Support 5V to 3.3V Band Gap Regulator for stable voltage supply
- Provide Over-Current protection mechanism for safety power supply
- On-Chip power MOSFETs for supplying flash media card power
- Support Power Saving mode/ Selective suspend mode for better power management.

  Only available in QFN-24(A) package.
- Support external serial EEPROM interface for the flexibility to load the vendor information and system options
- Operating system supported: Windows 7/Vista32&64/XP/2000/Me/98/98SE, Mac OS 9.X/10.X, Linux Kernel 2.4.X/2.6.X
  - Pass Windows Vista/ Windows 7 (Submission ID: 1355289)
- USB-IF Logo (Submission TID: 40000940)
- Package available in 24 pin SSOP (209 mil) and 24 pin QFN (4x4 mm)

*Note1: GL823-08, -11 does not support MultiMediaCard™ (MMC)

Table 2.1 - Product Difference Overview

Package Type	Version	Power Source	Power Management
SSOP 24	04, 06, …N	5V	Not Support
QFN-24 (A)	04, 06, …N	3.3V	Power Saving Mode/ Selective Suspend Mode
QFN-24 (B)	05, 07, …N+1	5V	Not Support

CHAPTER 3 PIN ASSIGNMENT

3.1 SSOP-24 Pinout

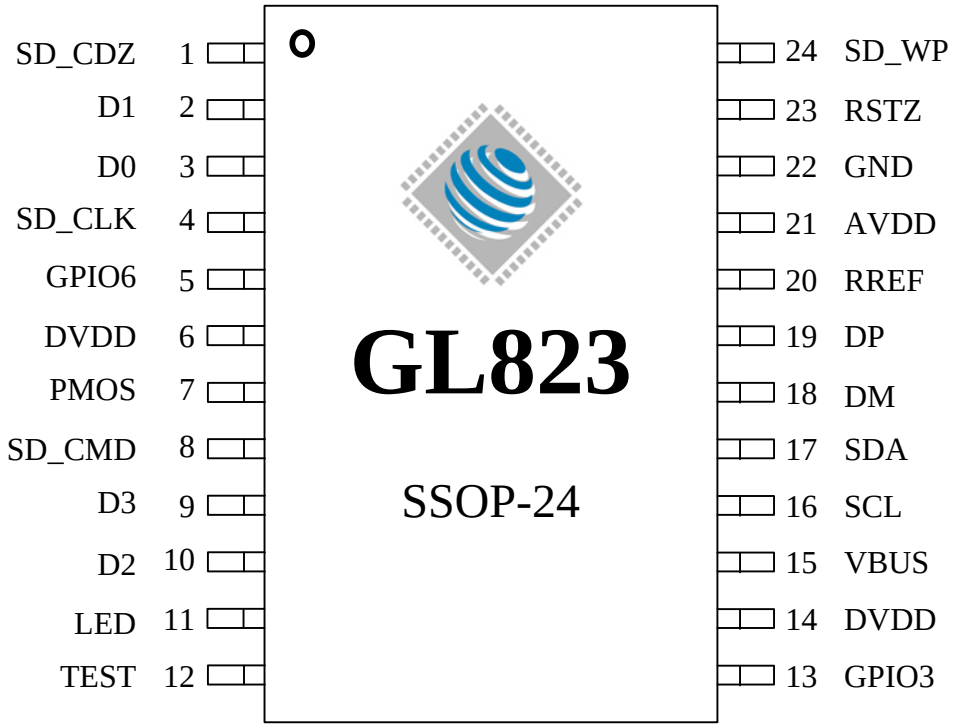


Figure 3.1 - 24 Pin SSOP Pin out Diagram

3.2 QFN-24 Pinout

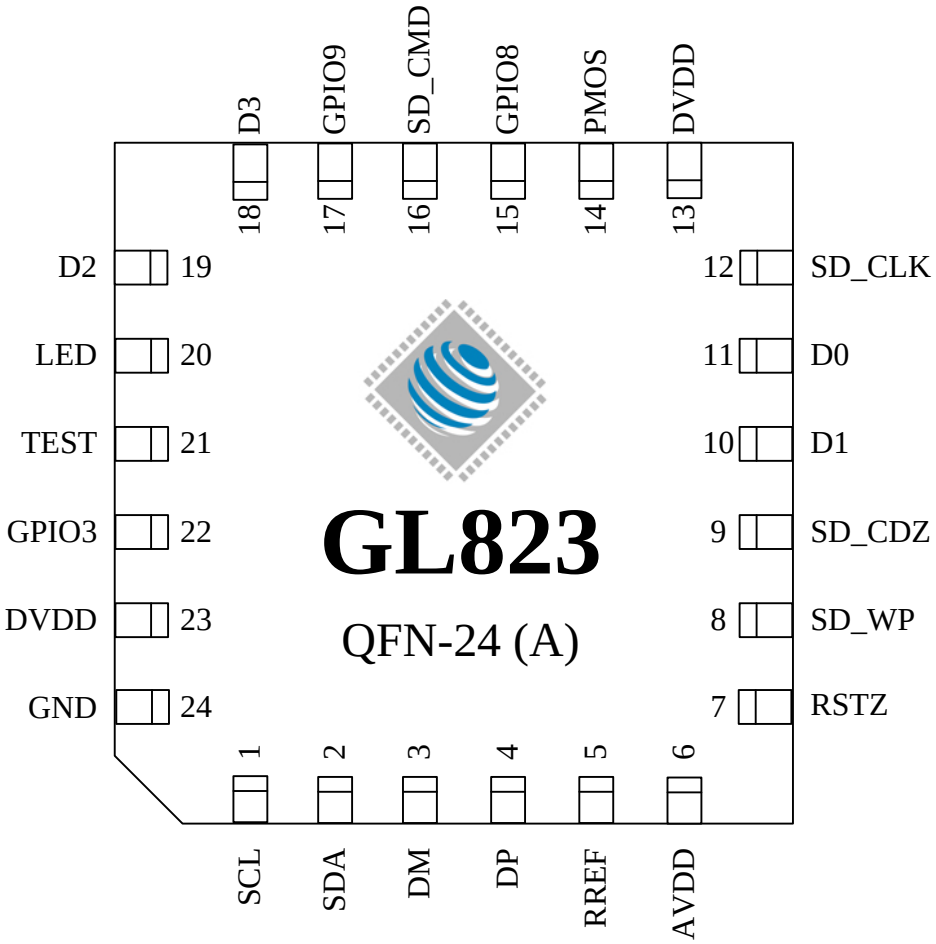


Figure 3.2 - 24 Pin QFN (A) Pin out Diagram

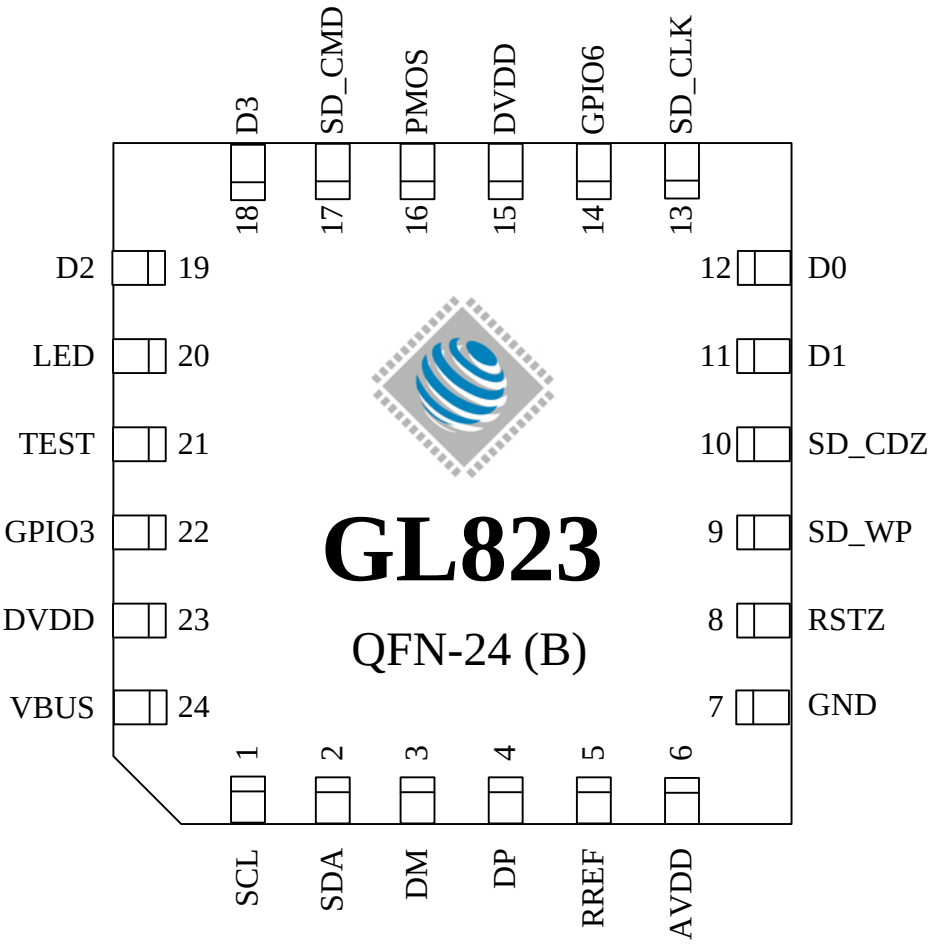


Figure 3.3 - 24 Pin QFN (B) Pin out Diagram

3.3 Pin List/Descriptions

Table 3.1 - GL823 Pin List/Descriptions

Pin Name	SSOP 24 pin	QFN 24 pin (A)	QFN 24 pin (B)	Type	Description
Power/Ground					
DVDD	6, 14	13,23	15,23	P	3.3V Digital power
AVDD	21	6	6	P	3.3V Analog power
VBUS	15	-	24	P	5V Power source
GND	5, 22	24	7	P	Ground
PMOS	7	14	16	P	Card power: 300mA, Drain-Source On-Resistance (R_{DS})= 1Ω (Max.) @3.3V, 25°C
G1	-	Die Pad	Die Pad	P	Ground
USB PHY Interface					
DM	18	3	3	A	USB D-
DP	19	4	4	A	USB D+
RREF	20	5	5	A	USB reference resistor. This pin is used to control the level of USB signal. A 680Ohm, 1% resistor is recommended to be laid between RREF and GND
SD Card Interface					
SD_WP	24	8	9	I, pu	SD Write Protect signal 0: Write enable 1: Write protect
SD_CDZ	1	9	10	I, pu	SD/MMC Card Detect signal 0: Card insert 1: No card
SD_CLK	4	12	13	O	SD/MMC Clock signal
SD_CMD	8	16	17	B, pu	SD/MMC Command signal
D[3:0]	9, 10, 2, 3	18,19,10,11	18,19,11,12	B, pu	SD/MMC Data signal
Others					
RSTZ	23	7	8	I, pu	This pin is used to reset the chip, active-low
TEST	12	21	21	I, pd	This pin is used to test the chip. 0: Normal operation 1: Test mode
GPIO3	13	22	22	B	Hardware configuration
GPIO6	5	-	14	B	Hardware configuration
GPIO8	-	15	-	B	Hardware configuration
GPIO9	-	17	-	B	Hardware configuration
LED	11	20	20	O	Power & Access LED
SCL	16	1	1	B	Serial EEPROM Clock signal
SDA	17	2	2	B	Serial EEPROM Data signal

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	Internal pull-up when input
	pd	Internal pull-down when input
	P	Power / Ground
	A	Analog

Note:

1. AVDD connect to DVDD through Bead

2. All I/O pads are Schmitt trigger and 8mA drive current

CHAPTER 4 BLOCK DIAGRAM

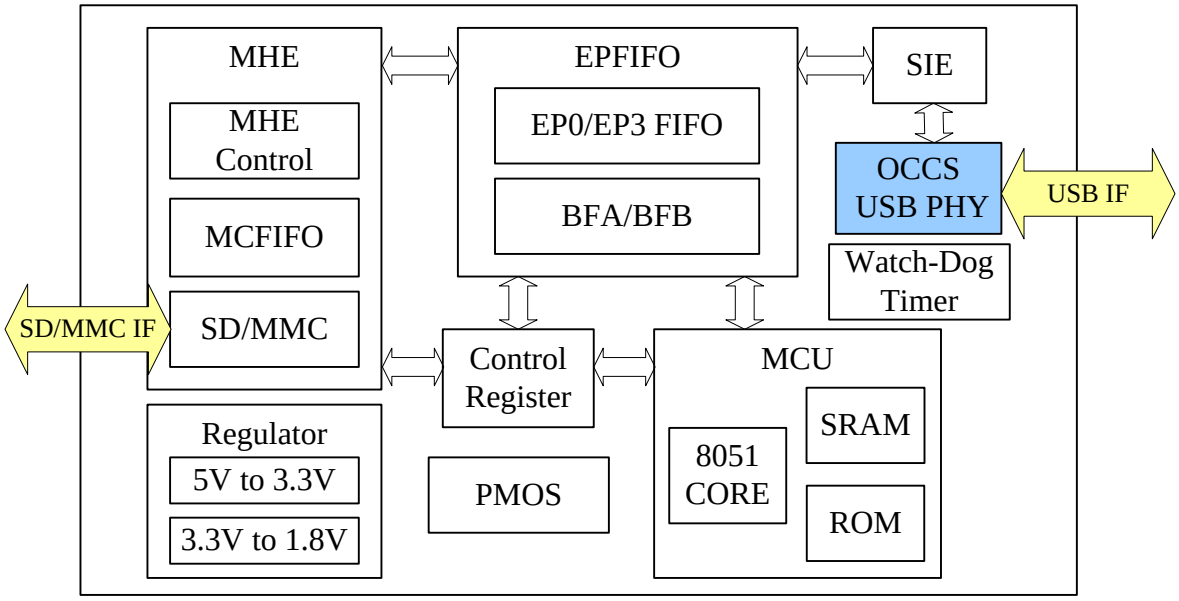


Figure 4.1 - Functional Block Diagram

4.1 OCCS USB PHY

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic. On chip clock source and no need of 12MHz Crystal Clock input.

4.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFOA/B)

- **Control FIFO** FIFO of control endpoint 0. It is 64-byte FIFO and used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by uC

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** FW code on ROM
- **SRAM** Internal RAM area for MCU access

4.5 MHE

- **MIF** Media Interface: SD/MMC
- **MCFIFO** It can access by MCU for memory card short data packet.

4.6 Regulator

- **5V to 3.3V** Band Gap Regulator for stable voltage supply for USB PHY, PMOS.
  When Power source is 3.3V, the 5V to 3.3V regulator will be disabled.
- **3.3V to 1.8V** For core logic and internal memory.

4.7 PMOS

On-Chip power MOSFETs provide Over-Current protection mechanism.

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Temperature Conditions

Table 5.1 – Temperature Conditions

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to 70 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter		Value
Supply Voltage	SSOP-24 & QFN-24(B)	4.75V to 5.25V
	QFN-24(A)	3.14V to 3.46V
Ground Voltage		0V

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
V5	Supply Voltage for SSOP-24 & QFN-24(B)		5V power source	4.75	-	5.25	V
V3.3	Supply Voltage for QFN-24(A)		3.3V power source	3.14	-	3.46	V
V_{IH}	Input High Voltage			2.0	-	-	V
V_{IL}	Input Low Voltage			-	-	0.4	V
I_I	Input Leakage Current		$0 < V_{IN} <$ DVDD	-10	-	10	µA
V_{OH}	Output High Voltage		DVDD = 3.3V	3.0	-	-	V
V_{OL}	Output Low Voltage			-	-	0.4	V
I_{OH}	Output Current High			-	8	-	mA
I_{OL}	Output Current Low			-	8	-	mA
C_{IN}	Input Pin Capacitance			-	5	-	pF
I_{NORMAL}	AVDD Supply current		5V/3.3V power source	-	33	-	mA
	DVDD Supply current			-	16	-	mA
I_{RESET}	AVDD Reset current		5V/3.3V power source	-	38	-	mA
	DVDD Reset current			-	11	-	mA
I_{SUS}	Suspend current	SSOP-24 & QFN-24(B)	1.5K pull-up included	-	-	450	µA
		QFN-24(A)		-	-	300	µA

I_{PS}	Power saving current	SSOP-24 & QFN-24(B)		-	-	200	μA
		QFN-24(A)		-	-	30	μA
R_{pu}	Reset Pad pull-up			-	10	-	KΩ
	SD_CMD/GPIO Pad pull-up			-	20	-	KΩ
	SD_DATA Pad pull-up			-	50	-	KΩ
R_{pd}	SD_CMD/GPIO Pad pull-down			-	20	-	KΩ
	SD_DATA Pad pull-down			-	50	-	KΩ
T_j	Absolute maximum junction temperature			0		125	℃

5.4 5V to 3.3V Regulator Characteristics

Table 5.4 - Regulator Output Current

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Unit
Iq	Quiescent current	No loading	-	18	-	uA
Io	Output driving capability	DVDD > 3.2V	-	-	350	mA
Io_0mA	DVDD without loading		-	3.38	-	V
Io_200mA	DVDD with 200mA loading		-	3.31	-	V
Io_350mA	DVDD with 350mA loading		-	3.24	-	V

(VBUS = 5V, Temperature 25 °C)

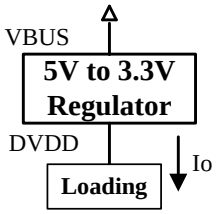


Figure 5.1 - 5V to 3.3V Regulator Architecture

5.5 PMOS Characteristics

Table 5.5 - PMOS I-V Table

Driving Loading (I)	PMOS Output Voltage
100mA	**3.21V**
200mA	**3.12V**
300mA	**3.01V**
330mA	**Turn Off ***

(DVDD = 3.3V, Temperature 25 °C)

Note:
PMOS turn off by over-current protection mechanism when loading over 330mA.

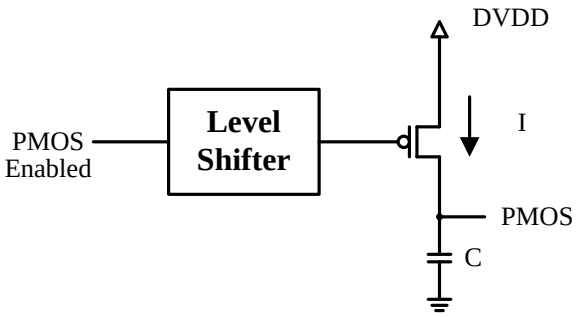


Figure 5.2 - Embedded PMOS Switch Architecture

5.6 AC Characteristics

5.6.1 Reset Timing

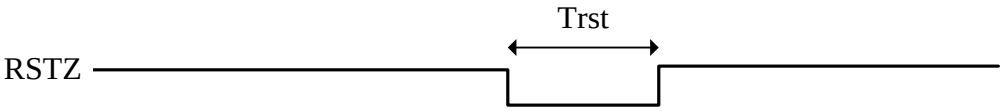


Figure 5.3 - Timing Diagram of Reset Width

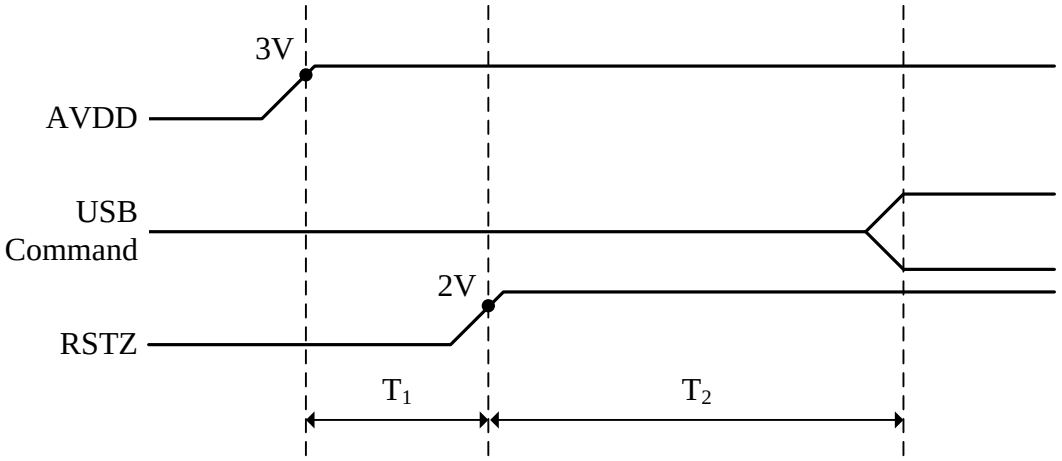


Figure 5.4 - Timing Diagram of Power Good to USB Command Receive Ready

Table 5.6 - Reset Timing

Parameter	Description	Min.	Unit
Trst	Chip reset sense timing width	2	us
T_1	AVDD power up to reset de-assert	500	us
T_2	Reset de-assert to respond USB command ready	42	ms

5.6.2 SD/MMC Card Clock Frequency

Table 5.7 - SD/MMC Card Clock Frequency

Parameter	Description	Typ.	Unit
F_{ID}	Clock frequency Identification Mode	387	KHz
F_{DS}	Clock frequency Default Speed Mode	24	MHz
F_{HS}	Clock frequency High Speed Mode	48	MHz

CHAPTER 6 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	2.00 (79)
A1	0.05 (2)	---	---
A2	1.65 (65)	1.75 (69)	1.85 (73)
b	0.22 (9)	---	0.38 (15)
c	0.09 (4)	---	0.25 (10)
D	7.90 (311)	8.20 (323)	8.50 (345)
E	7.40 (291)	7.80 (307)	8.20 (323)
E1	5.00 (197)	5.30 (209)	5.60 (220)
e	0.65 (26) BSC		
L	0.55 (22)	0.75 (30)	0.95 (37)
L1	1.25 (49) REF		
Y	---	---	0.10 (4)
θ	0°	4°	8°

NOTE: 1. REFER TO JEDEC MS-150
2. CONTROLLING DIMENSIONS : MILLIMETER

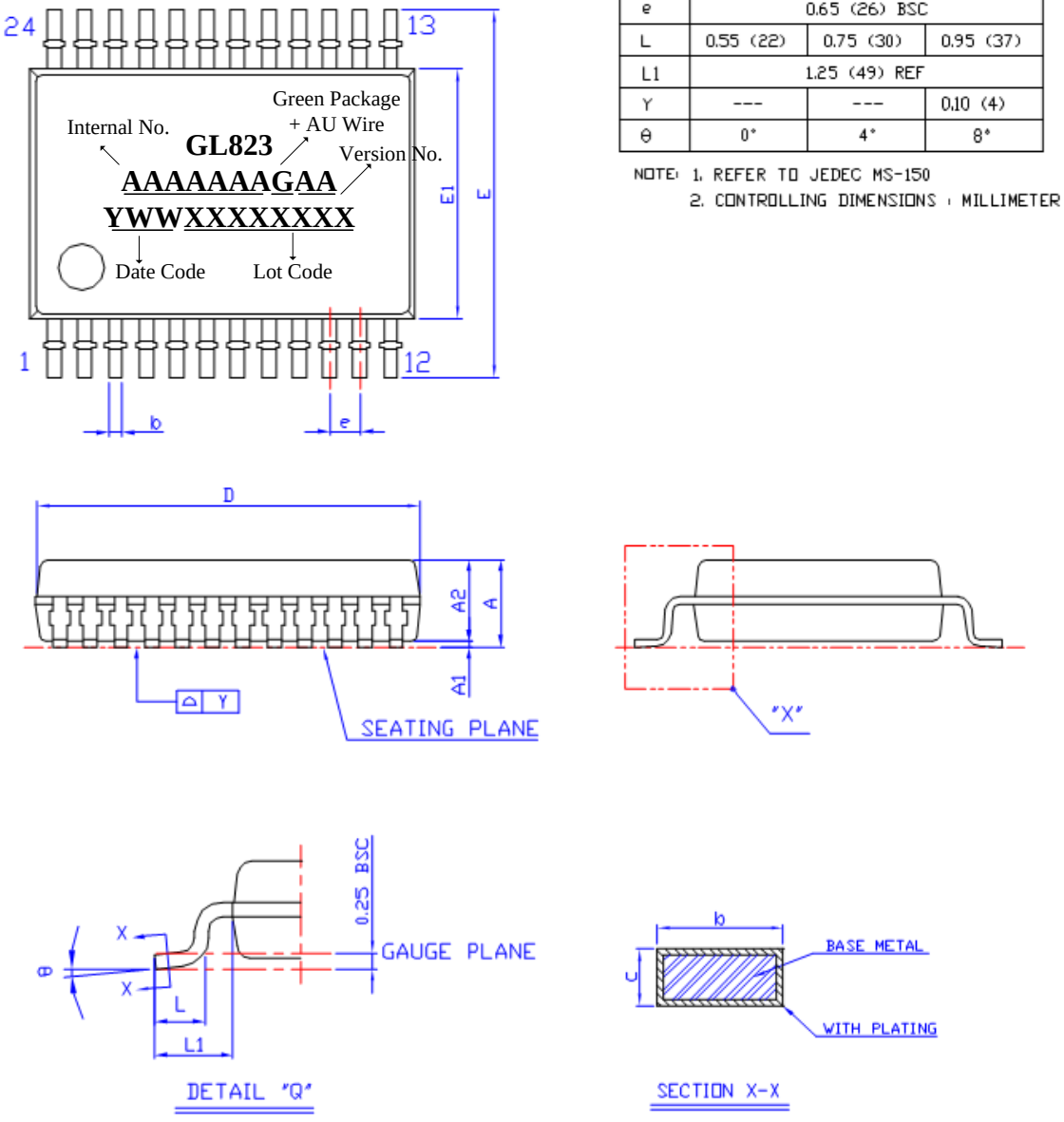
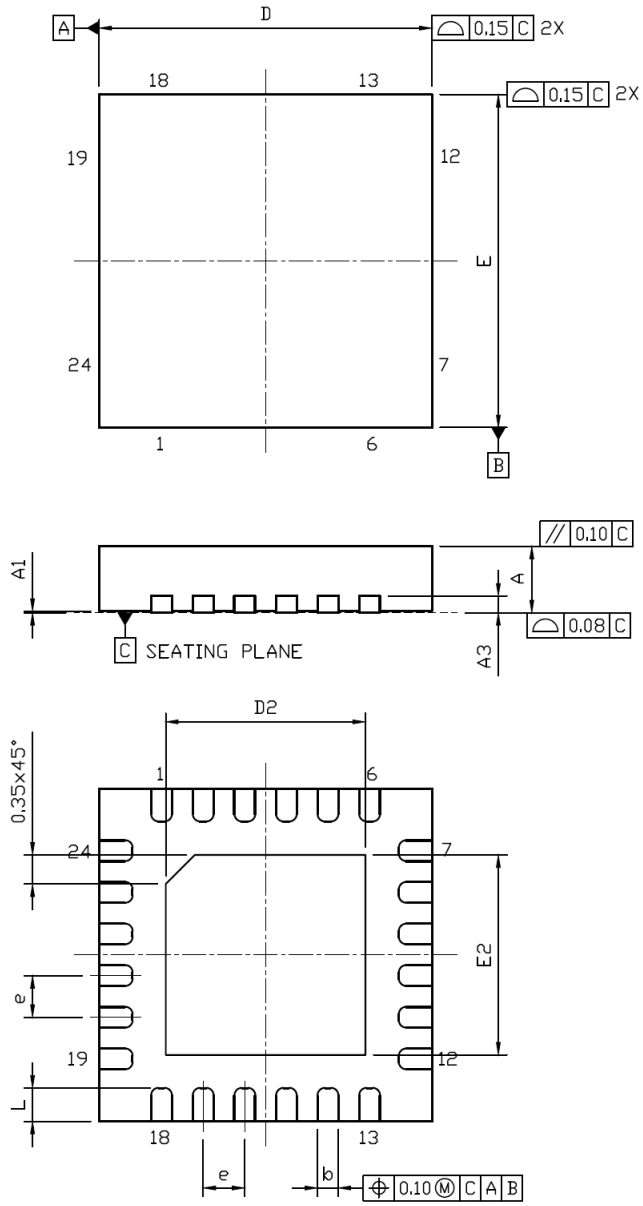


Figure 6.1 - SSOP 24 Pin Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	4.00 (157.4) BSC		
D2	1.90 (74.8)	2.40 (94.5)	2.85 (112.2)
E	4.00 (157.4) BSC		
E2	1.90 (74.8)	2.40 (94.5)	2.85 (112.2)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 6.2 - QFN 24 Pin Package

CHAPTER 7 ORDERING INFORMATION

Table 7.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL823-HGGXX	SSOP 24	Green Package + AU Wire	XX	Available
GL823-OGG*XX	QFN 24	Green Package + AU Wire	XX	Available
GL823-OGY*XX	QFN 24	Green Package + CU Wire	XX	Available

*The marking of "OGG" and “OGY” will not be shown on the IC due to QFN 24 package size limitation.