DATA SHEET

Generalplus

GPM8F3331B

48 / 32 Pin 8-bit Microcontroller with 32KB Flash

Preliminary

Aug. 24, 2021

Version 0.3

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48 / 32 PIN 8-BIT MICROCONTROLLER WITH 32KB FLASH

1. GENERAL DESCRIPTION

GPM8F3331B, a highly integrated microcontroller, features a pipelined 1T 8051-based CPU, 3K-byte XRAM, 256-byte IDM SRAM, and 32K-byte program FLASH into a single chip. It supports up to 29 programmable multi-functional I/Os, Timer0/1/A/B/C, UART0 ,SPI, I2C (master/slaver), three internal gain OPs, two comparators, 65.3824MHz PLL, XTAL8M , IOSC32K and one 13-channle SAR ADC with 12-bit resolution. GPM8F3331B operates over a wide voltage range of 2.4V - 5.5V with variety of clock sources and features one power saving mode in power management unit to manage power consumption efficiently. Moreover, there is an on-chip debug circuit with two pins equipped to facilitate a full speed in-system debug during application development phase.

2. FEATURES

- **CPU**
  - High speed and high performance 1T 8051-based CPU
    - 100% software compatible with industry standard 8051
    - Pipeline RISC architecture to execute instructions 10 times faster than standard 8051
    - Up to 65.3824MHz clock operation
- **Memory**
  - 3K bytes XRAM
  - 256 bytes internal Data Memory (IDM) SRAM
  - 32K bytes FLASH with high endurance
    - Minimum 100,000 program/erase cycles
    - Minimum 10 years data retention
    - 512-byte page size
  - Programmable read only level for software security
- **Clock Management**
  - Internal oscillator: 8MHz±2% @ 2.4V~5.5V
  - Internal oscillator with PLL: 65.3824 / 63.85 / 60.019 / 52.357 MHz
  - Crystal input with 8MHz
  - Internal oscillator: 32KHz ± 50% @ 2.4V~5.5V
- **Power Management**
  - One Sleep mode for power saving
- **Interrupt Management**
  - 12 interrupt sources
  - Two external interrupt sources
- **Reset Management**
  - Power On Reset (POR)
  - Low Voltage Reset (LVR)
  - Pad Reset (PAD_RST)
  - Watchdog Reset (WDT_RST)
  - Software Reset (S/W_RST)
  - FLASH Access Error Reset (ADDR_ERR_RST)
- **Programmable Watchdog Timer**
  - A time-base generator
  - An event timer
  - System supervisor
- **Three Ops**
  - Internal gain included
  - Resistance between OP_O and CMP_N/ CMP_P input path included
- **Two Comparator**
  - Programmable hysteresis and de-bounce select
  - Programmable input source select.
- **I/O Ports**
  - Up to 29 multifunction bi-direction I/Os
  - Each incorporates with pull-up resistor, pull-down resistor, output high, output low , output driving capability and floating input, determined by user's settings at the corresponding registers
  - I/O ports with 15mA or 8mA current sink @ VDD = 5V
  - I/O ports with 15mA or 8mA current drive @ VDD = 5V
- **Two 16-bit Timers/Counters (Timer 0/1)**
  - Timer mode with selectable clock sources
  - Auto reload 8-bit timers
- **Three Powerful Timers: TimerA / TimerB / TimerC, with 16-bit Compare / Capture / PWM Unit**
  - Timer mode with selectable clock source
  - Auto-reload 16-bit timers
  - Event capturing
  - Pulse width modulation and measurement
  - TimerA providing 4 channels PWM/Capture
  - TimerB providing 2 channels PWM/Capture
  - TimerC providing 2 channels Capture
- **UART0**
  - One synchronous mode
  - Three asynchronous modes
- **SPI (master / slaver mode)**
  - Programmable phase and polarity of master clock
  - Programmable master SPI clock frequency
- **I2C (master / slaver mode)**
  - Programmable master I2C clock frequency
  - Max I2C clock: 400 KHz
- **A/D Converter**
  - One 13-channel 12-bit resolution ADC
  - Supports programmable sample & hold and ADC clock

function
- Control independent per set
- Internal VSS channel
- Offset calibration
- Direct memory access from ADC to XRAM

- **Built-in Low Voltage Reset**
  - Trigger level: 2.4V, 2.8V, 3.2V, 4.2V
- **Built-in Low Voltage Detection**
  - Programmable level: 2.6V, 3.0V, 3.4V, 4.4V
- **On-chip Debug Unit**
  - C compatible development tools

Product Number	GPM8F3331B	
Package Type	QFN32	LQFP48
Max System Clock (MHz)	65.3824	65.3824
Operating Voltage (V)	2.4~5.5	2.4~5.5
FLASH (Kbytes)	32	32
XRAM (bytes)	3K	3K
IDM (bytes)	256	256
Timer (sets)	5	5
UART	1	1
SPI	--	1
I2C (master / slaver)	1	1
Built-in OP (sets)	3	3
Built-in Comparator(sets)	2	2
13-Channel 12-bit ADC (sets)	1	1
IO	24	29

3. BLOCK DIAGRAM

3.1. GPM8F3331B

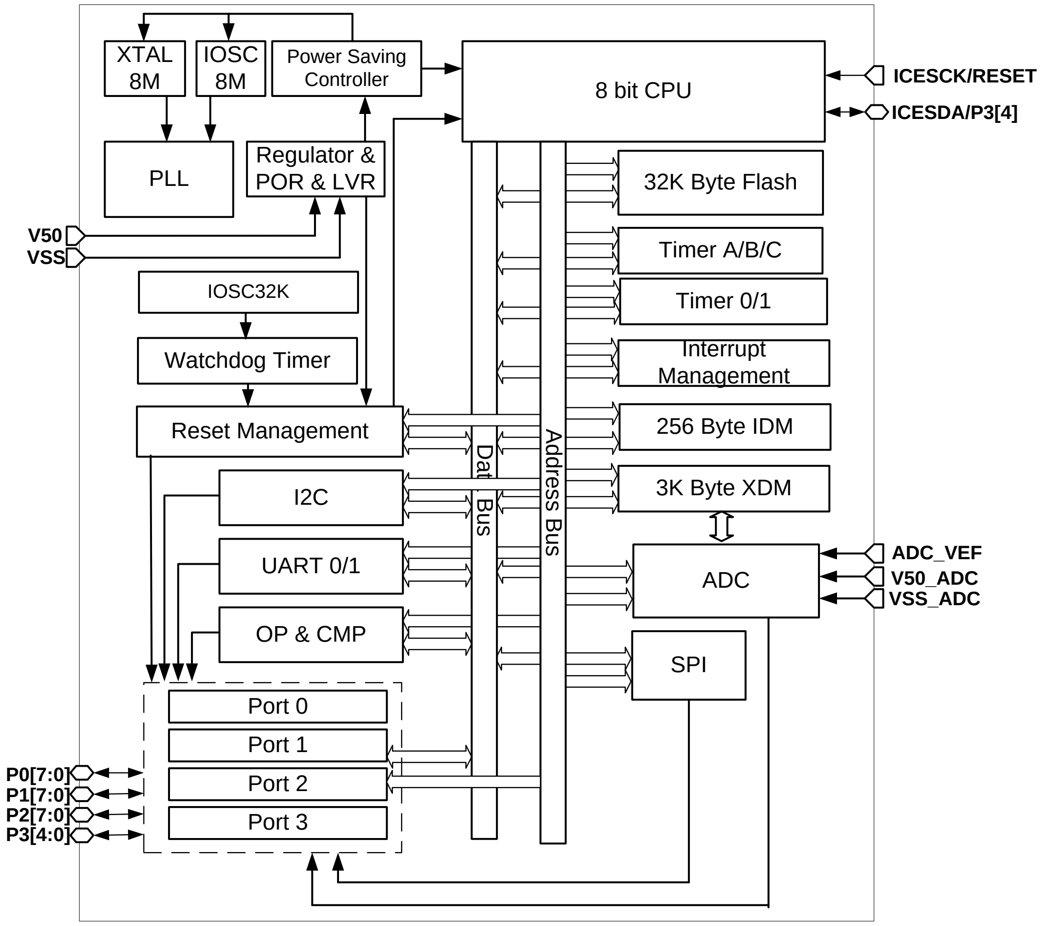


Figure 3-1 Block diagram of GPM8F3331B

4. SIGNAL DESCRIPTIONS

4.1. Pin Descriptions

4.1.1. GPM8F3331B

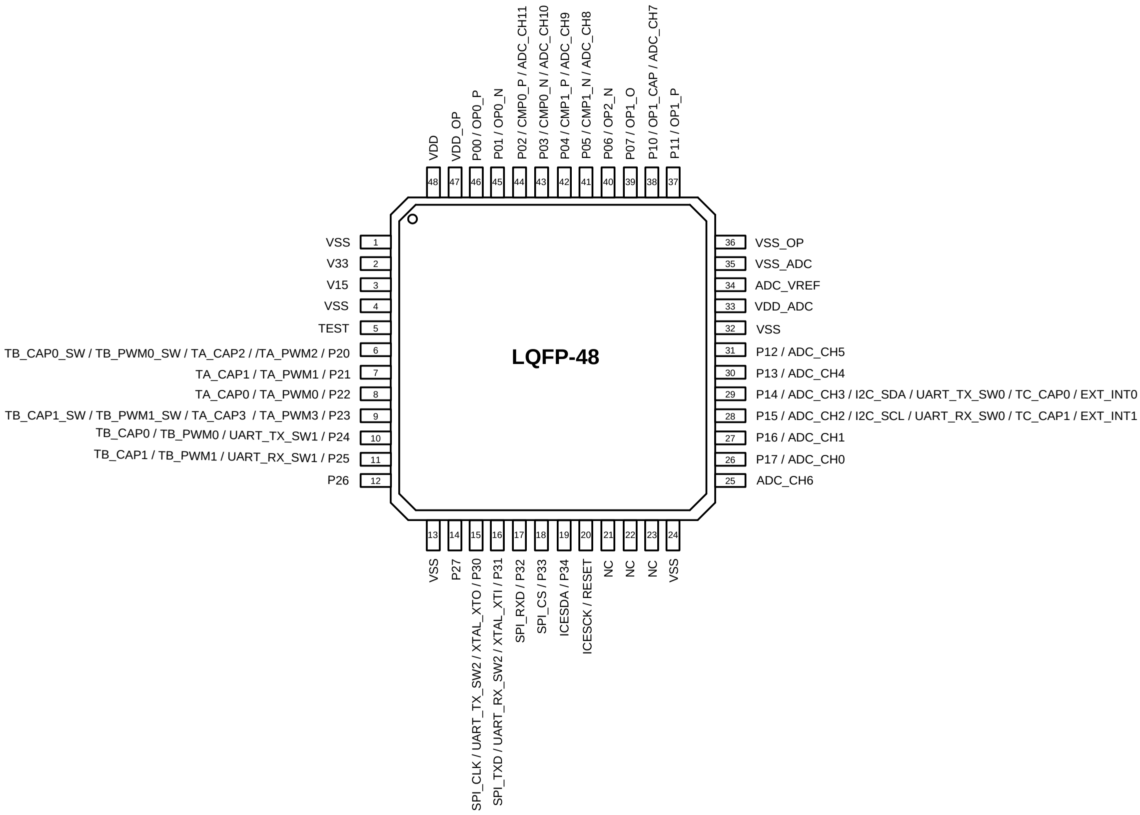
Type：I = Input, O = Output, P = Power , G = GND

Pin Name	LQFP48	QFN32	Type	Description
VSS	1	--	G	Ground Pin
V33	2	--	P	V33 Regulator Output Power Pin
V15	3	4	P	V15 Regulator Output Power Pin
VSS	4	33	G	Ground Pin
Test	5	--	I	Test Pin
P20	6	5	I/O	Port 2's bit 0 / TMAPWM2/ TMACAP2 / TBPWM0_SW
P21	7	6	I/O	Port 2's bit 1 / TMAPWM1/ TMACAP1
P22	8	7	I/O	Port 2's bit 2 / TMAPWM0/ TMACAP0
P23	9	8	I/O	Port 2's bit 3 / TMAPWM3/ TMACAP3 / TBPWM1_SW
P24	10	9	I/O	Port 2's bit 4 / TBPWM0 / UART_TX_SW1
P25	11	--	I/O	Port 2's bit 5 / TBPWM1 / UART_RX_SW1
P26	12	--	I/O	Port 2's bit 6
VSS	13	--	G	Ground Pin
P27	14	--	I/O	Port 2's bit 7
P30	15	10	I/O	Port 3's bit 0 / UART_TX_SW2 / XTO / SPI_CLK
P31	16	11	I/O	Port 3's bit 1 / UART_RX_SW2 / XTI / SPI_TXD
P32	17	--	I/O	Port 3's bit 2 / SPI_RXD
P33	18	--	I/O	Port 3's bit 3 / SPI_CS
P34	19	12	I/O	Port 3's bit 4 / ICE_SDA
RESET	20	13	I	Reset Pin (high active) / ICE_SCK
VSS	24	--	G	Ground Pin
ADC_IN	25	14	I	ADC_Channel 6
P17	26	15	I/O	Port 1's bit 7 / ADC_Channel 0
P16	27	16	I/O	Port 1's bit 6 / ADC_Channel 1
P15	28	17	I/O	Port 1's bit 5 / ADC_Channel 2 / I2C_SCL / UART_RX_SW0 / TMC_CAP1 / EXT_INT1
P14	29	18	I/O	Port 1's bit 4 / ADC_Channel 3 / I2C_SDA / UART_TX_SW0 / TMC_CAP0 / EXT_INT0
P13	30	19	I/O	Port 1's bit 3 / ADC_Channel 4
P12	31	20	I/O	Port 1's bit 2 / ADC_Channel 5
VDD_ADC	33	21	P	Analog ADC Power Pin
ADC_VREF	34	22	P	Analog ADC Regulator Output Pin
VSS_ADC	35	23	G	Analog ADC Ground Pin / ADC_Channel 12
VSS_OP	36	24	G	Analog OP Ground Pin
P11	37	25	I/O	Port 1's bit 1 / OP1_P
P10	38	26	I/O	Port 1's bit 0 / ADC_Channel 7 / OP1_CAP
P07	39	27	I/O	Port 0's bit 7 / OP1_O
P06	40	28	I/O	Port 0's bit 6 / OP2_N
P05	41	29	I/O	Port 0 bit 5 / ADC_Channel 8 / CMP1_N
P04	42	30	I/O	Port 0's bit 4 / ADC_Channel 9 / CMP1_P
P03	43	31	I/O	Port 0's bit 3 / ADC_Channel 10 / CMP0_N

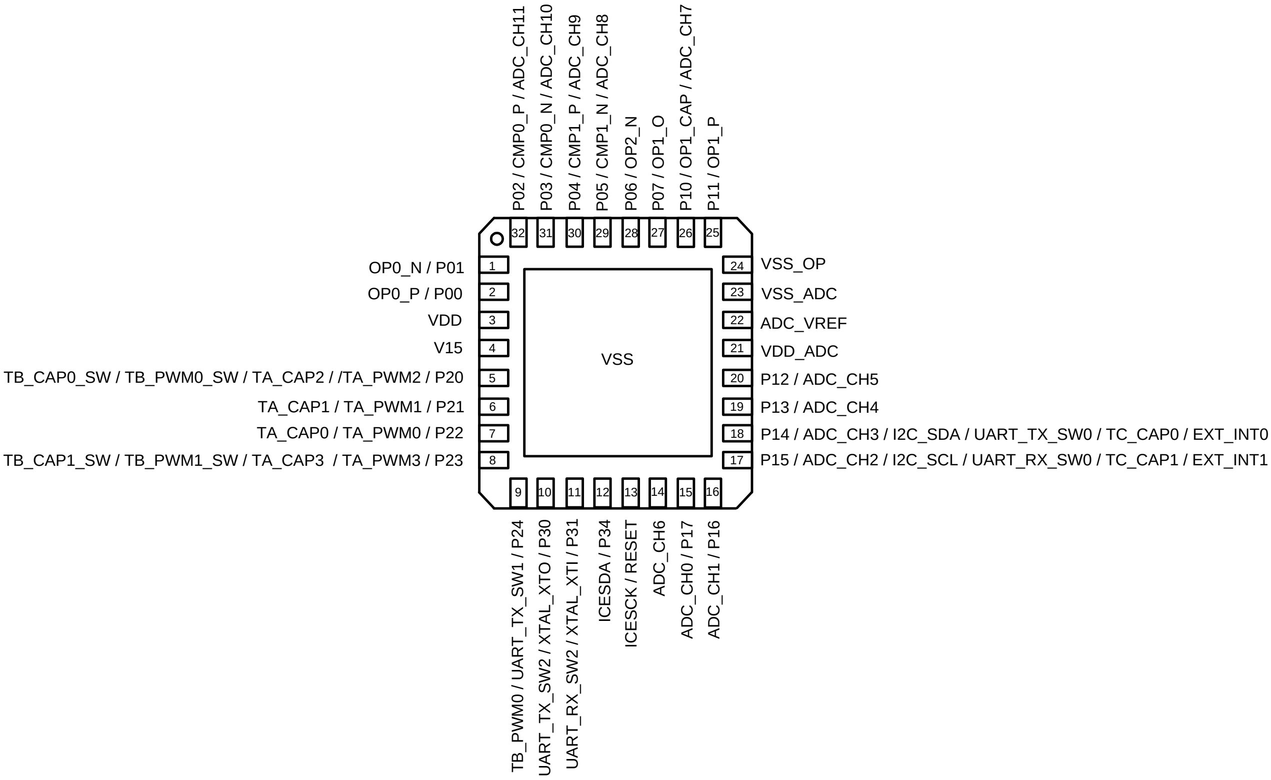
Pin Name	LQFP48	QFN32	Type	Description
P02	44	32	I/O	Port 0's bit 2 / ADC_Channel 11 / CMP0_P
P01	45	1	I/O	Port 0's bit 1 / OP0_N
P00	46	2	I/O	Port 0's bit 0 / OP0_P
VDD_OP	47	--	P	Analog OP Power Pin
VDD	48	3	P	V50 Power Pin

4.2. PIN Map

Package Pin Sequence – LQFP48 pin map



Package Pin Sequence – QFN32 pin map



5. FUNCTION DESCRIPTIONS

5.1. Central Processing Unit

5.1.1. CPU Introduction

The CPU is an ultra-high performance and high speed microcontroller. The pipelined architecture makes the CPU 10 times faster than the standard architecture. This performance can also be exploited to great advantage in low power application in which core can be clocked over ten times slower than original implementation without performance loss.

5.1.2. CPU Features

- 100 % software compatible with industry 8051 CPU
- 24 times faster multiplication
- 12 times faster addition

The CPU is fully compatible with industry standard 8051 microcontroller, maintaining all instruction mnemonics and binary compatibility. It incorporates some great architectural enhancements, allowing the CPU instructions execution with high performance and high speed.

The arithmetic section of the processor performs extensive data manipulation and is comprised of an 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

5.1.3. Arithmetic Logic Unit (ALU)

The ALU performs the arithmetic and logic operations during one instruction execution. Typical arithmetic operations are addition, subtraction, multiplication and division. Additional operations are such as increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit, operation such as AND, OR, Exclusive OR, complement and rotation are performed. The Boolean processor performs the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to from carry.

5.1.4. Accumulator (A register)

The accumulation is the 8-bit general-purpose register, which can be operated with data transfer, temporary saving, condition judgment, etc.

5.1.5. B register

The B register is used during multiply and divide operations. In other cases, it may be used as normal SFR.

5.1.6. Program Status Word (PSW)

The PSW contains several bits that reflect the current state of the CPU which is similar to the flag-register of general CPU.

5.1.7. Program Counter (PC)

The program counter is a 16-bit wide register. It consists of two 8-bit registers: PCH and PCL. This register indicates the address of next instruction to be executed. In Reset state, the content of 0x0000 is stored into program counter.

ACC			**Address: 0xE0**		**Accumulator A Register**			
Bit	7	6	5	4	3	2	1	0
Function	ACC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	ACC[7:0]	R/W	Accumulator A	

Table 5-1 The ACC register

B			**Address: 0xF0**		**B Register**			
Bit	7	6	5	4	3	2	1	0
Function	B[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	B[7:0]	R/W	B	

Table 5-2 The B register

PSW			Address: 0xD0		Program Status Word Register			
Bit	7	6	5	4	3	2	1	0
Function	CY	AC	F0	RS1	RS0	OV	F1	P
Default	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7</td><td>CY</td><td>R/W</td><td>Carry flag</td><td></td></tr>
<tr><td>6</td><td>AC</td><td>R/W</td><td>Auxiliary carry flag</td><td></td></tr>
<tr><td>5</td><td>F0</td><td>R/W</td><td>General purpose flag 0</td><td></td></tr>
<tr><td>4:3</td><td>RS[1:0]</td><td>R/W</td><td>Register bank select bits<table><tr><th>RS[1:0]</th><th>Function description</th></tr><tr><td>00</td><td>Bank 0, data address 0x00-0x07</td></tr><tr><td>01</td><td>Bank 1, data address 0x08-0x0F</td></tr><tr><td>10</td><td>Bank 2, data address 0x10-0x17</td></tr><tr><td>11</td><td>Bank 3, data address 0x18-0x1F</td></tr></table></td><td></td></tr>
<tr><td>2</td><td>OV</td><td>R/W</td><td>Overflow flag</td><td></td></tr>
<tr><td>1</td><td>F1</td><td>R/W</td><td>General purpose flag 1</td><td></td></tr>
<tr><td>0</td><td>P</td><td>R/W</td><td>Parity flag</td><td></td></tr>
</table>

Table 5-3 The PSW register

5.2. Memory Organization

5.2.1. Introduction

GPM8F3331B has three separated address spaces for program memory and data memory. The program memory is on-chip, re-programmable FLASH memory and contains up to 32K bytes spaces. The data memory is 3K bytes of external RAM, 256 bytes IDM with 128 bytes x 4 pages of SFR which can be read and written. The upper IDM and SFR use the same access address in different access ways which are described in **Figure 5-2**.

5.2.2. Program Memory Allocation

The program memory size is 32KB. If system clock is set to PLL out with 65.3824MHz, CPU and peripheral will operate in 16.3456MHz frequency and 65.3824MHz respectively. In the code area, the address 0x008F is used for CONFIG_BYTE whose definition of each bit is described in Table 5-4. User can lock the program or content by setting CONFIG_BYTE[0]. If CONFIG_BYTE[0] is programmed to be '0' , the whole chip memory is protected and any page erase or programming by two wire serial interface is not allowed. The only thing user can do is to erase whole chip. Figure **5-1** shows the program memory map of 32KB FLASH.

After each reset, CPU starts execution in the program memory at location 0x0000. Each interrupt has its own start address for service routine. The FLASH memory can be programmed in-system, through the ICESCK/ICESDA interface or by software using the MOVX instruction when PWE= 1. User can refer to the example code in the programming guide for the procedure of write and erase operations. FLASH data cannot be programmed from a '0' to '1', and only erase operation can be accepted. Therefore, FLASH data is erased (set to 0xFF) before being programmed. The write and erase operations are executed by using Pseudo-idle mode to be automatically timed by hardware without data polling to determine the end of the write and erase operation.

For software security consideration, user can set the programmable FLASH level by FLH_CTRL1 register to limit the code area that avoids inadvertently erased or written by software; the protected region is called READONLY_PAGE.

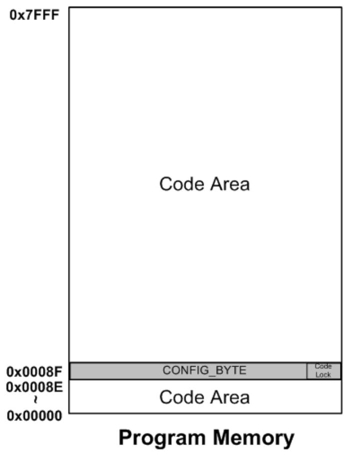


Figure 5-1 Program memory organization

CONFIG_BYTE			Address: 0x8F (Code Area)		CONFIG_BYTE Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	--	CODE Lock
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:1	--	R	Reserved	
0	CODE Lock	R	0: CODE locked; 1: CODE unlocked	

Table 5-4 The CONFIG_BYTE register

FLH_CTRL0			Common / Address: 0xEC		FLASH Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	FLH_PERASE	FLH_PROG
Default	1	1	1	1	1	1	0	0
Key Code	0x8F, 0x32 , 0x51							

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	FLH_PERASE	R/W	FLASH page erase enable bit 0: FLASH page erase disabled 1: FLASH page erase enabled	
0	FLH_PROG	R/W	FLASH program enable bit. 0: FLASH program disabled 1: FLASH program enabled	

Table 5-5 The FL_LEVELLASH_CTRL0 register

FLH_CTRL1			Common / Address: 0xED		FLASH Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	FLASH_LEVEL[4:0]				
Default	1	1	1	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x51							

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:5</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>4:0</td><td>FLASH_LEVEL[4:0]</td><td>R/W</td><td>FLASH_LEVEL, it determines how many 1K pages are read only
<table>
<tr><th>FLASH_LEVEL</th><th>Note</th></tr>
<tr><td>0</td><td>no page is read only</td></tr>
<tr><td>1</td><td>address < 0x800 is read only</td></tr>
<tr><td>2</td><td>address < 0xC00 is read only</td></tr>
<tr><td>3</td><td>address < 0x1000 is read only</td></tr>
<tr><td>4</td><td>address < 0x1400 is read only</td></tr>
<tr><td>5</td><td>address < 0x1800 is read only</td></tr>
<tr><td>6</td><td>address < 0x1C00 is read only</td></tr>
<tr><td>7</td><td>address < 0x2000 is read only</td></tr>
<tr><td>8</td><td>address < 0x2400 is read only</td></tr>
<tr><td>9</td><td>address < 0x2800 is read only</td></tr>
<tr><td>10</td><td>address < 0x2C00 is read only</td></tr>
<tr><td>11</td><td>address < 0x3000 is read only</td></tr>
<tr><td>12</td><td>address < 0x3400 is read only</td></tr>
<tr><td>13</td><td>address < 0x3800 is read only</td></tr>
<tr><td>14</td><td>address < 0x3C00 is read only</td></tr>
<tr><td>15</td><td>address < 0x4000 is read only</td></tr>
<tr><td>16</td><td>address < 0x4400 is read only</td></tr>
<tr><td>17</td><td>address < 0x4800 is read only</td></tr>
<tr><td>18</td><td>address < 0x4C00 is read only</td></tr>
<tr><td>19</td><td>address < 0x5000 is read only</td></tr>
<tr><td>20</td><td>address < 0x5400 is read only</td></tr>
<tr><td>21</td><td>address < 0x5800 is read only</td></tr>
<tr><td>22</td><td>address < 0x5C00 is read only</td></tr>
<tr><td>23</td><td>address < 0x6000 is read only</td></tr>
<tr><td>24</td><td>address < 0x6400 is read only</td></tr>
<tr><td>25</td><td>address < 0x6800 is read only</td></tr>
<tr><td>26</td><td>address < 0x6C00 is read only</td></tr>
<tr><td>27</td><td>address < 0x7000 is read only</td></tr>
<tr><td>28</td><td>address < 0x7400 is read only</td></tr>
<tr><td>29</td><td>address < 0x7800 is read only</td></tr>
<tr><td>30</td><td>Prohibit</td></tr>
<tr><td>31</td><td>Prohibit</td></tr>
</table>
Note 1: In GPM8F3331B, only 5-bit FLASH_LEVEL is available.</td><td></td></tr>
</table>

Table 5-6 The FLH_CTRL1 register

5.2.3. Data Memory Allocation

Data memory addresses allocates on the GPM8F3331B are divided into two parts. The first part is 3K bytes of external RAM and the second one is 256 byte IDM, as shown in Figure **5-2**. The lowest internal data memory (IDM) consists of four register banks with eight registers each. A bit addressable segment with 128 bits (16 bytes) begins at 0x20. The address from 0x30 to 0x7F is not defined and can be utilized freely by user. The last 128 bytes of data memory can be used by different addressing modes. With the indirect addressing mode, address from 0x80 to 0xFF shared with stack space is addressed. With the direct addressing mode, the SFR addressing from 0x80 to 0xFF is accessed. The SFR memory map is shown in **Table 5-7**.

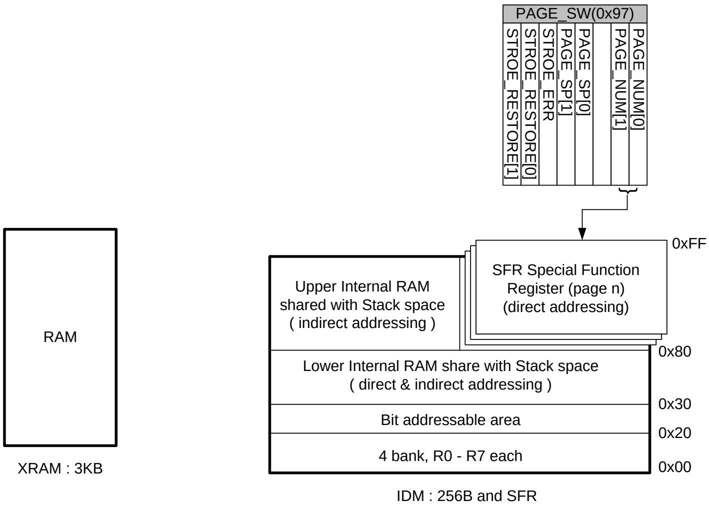


Figure 5-2 Data memory organization

Note1: Gray Area: common SFR register; White area: additional SFR register;
Note2: Switch page is unnecessary when user-defined gray area is written.

Page0	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP	SYS_CTRL0	SYS_CTRL1	SYS_CTRL2	SYS_CTRL3	SYS_CTRL4	SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved
0xE0	ACC	I2C_ADDR1	I2C_ADDR2	I2C_TXDATA	I2C_RXDATA	EXT_INT_EN	EXT_INT_EDGE	EXT_INT_FLAG
0xD8	WDCON	I2C_CTRL0	I2C_CTRL1	I2C_DEBOUNCE	I2C_STS0	I2C_STS1		
0xD0	PSW					Reserved	Reserved	Reserved
0xC8								
0xC0								
0xB8	IP	P1_ID	P1_DIR	P1_ATT	P1_DS	P1_SR	P1_SMT	
0xB0	P3	P3_ID	P3_DIR	P3_ATT	P3_DS	P3_SR	P3_SMT	
0xA8	IE	P0_ID	P0_DIR	P0_ATT	P0_DS	P0_SR	P0_SMT	
0xA0	P2	P2_ID	P2_DIR	P2_ATT	P2_DS	P2_SR	P2_SMT	
0x98	SCON0	SBUF0	SPI_CTRL	SPI_STS	SPI_TXD	SPI_RXD	BODY_ID0	BODY_ID1
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Page1	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP					CHARGE_CTRL	SYS_CTRL5	SYS_CTRL6
0xF0	B	OP_CTRL0	OP_CTRL1	OP_CTRL2		CMP_CTRL0	CMP_CTRL1	CMP_CTRL2
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved

0xE0	ACC							EXT_INT_FLAG
0xD8	WDCON							
0xD0	PSW					Reserved	Reserved	Reserved
0xC8								
0xC0								
0xB8	IP	P1_ID	ADC_DMA_TAR_ADDR_L	ADC_DMA_TAR_ADDR_H	ADC_OFSET_VAL			
0xB0	P3	P3_ID	ADC_WDG_HB_L	ADC_WDG_HB_H	ADC_WDG_LB_L	ADC_WDG_LB_H		
0xA8	IE	P0_ID	ADC_REG_SEQ3	ADC_REG_SEQ4	ADC_REG_SEQ5	ADC_REG_SEQ6		
0xA0	P2	P2_ID	ADC_CTRL6	ADC_REG_DATA_L	ADC_REG_DATA_H	ADC_REG_SEQ0	ADC_REG_SEQ1	ADC_REG_SEQ2
0x98	SCON0	SBUF0	ADC_CTRL0	ADC_CTRL1	ADC_CTRL2	ADC_CTRL3	ADC_CTRL4	ADC_CTRL5
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Page2	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved
0xE0	ACC							EXT_INT_FLAG
0xD8	WDCON							
0xD0	PSW					Reserved	Reserved	Reserved
0xC8			TMC_CAP1_L	TMC_CAP1_H	TMC_CAP2_L	TMC_CAP2_H	TMC_CAP3_L	TMC_CAP3_H
0xC0			TMC_CAP_CTRL1		TMC_CAP_INTEN	TMC_CAP_INTSTS	TMC_CAP0_L	TMC_CAP0_H
0xB8	IP	P1_ID	TMC_CTRL	TMC_PLOAD_L	TMC_PLOAD_H	TMC_L	TMC_H	TMC_CAP_CTRL0
0xB0	P3	P3_ID						
0xA8	IE	P0_ID	TMB_CCP0_L	TMB_CCP0_H	TMB_CCP1_L	TMB_CCP1_H		
0xA0	P2	P2_ID	TMB_CAP_CTRL1	TMB_CAP_INTCTR	TMB_PWM_CTRL0	TMB_PWM_CTRL1	TMB_PWM_DTIME	
0x98	SCON0	SBUF0	TMB_CTRL	TMB_PLOAD_L	TMB_PLOAD_H	TMB_L	TMB_H	TMB_CAP_CTRL0
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Page3	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved
0xE0	ACC							EXT_INT_FLAG
0xD8	WDCON							
0xD0	PSW					Reserved	Reserved	Reserved
0xC8			TMA_PWM2_END_L	TMA_PWM2_END_H	TMA_PWM3_END_L	TMA_PWM3_END_H		
0xC0					TMA_PWM0_END_L	TMA_PWM0_END_H	TMA_PWM1_END_L	TMA_PWM1_END_H
0xB8	IP	P1_ID						
0xB0	P3	P3_ID	TMA_CCP1_L	TMA_CCP1_H	TMA_CCP2_L	TMA_CCP2_H	TMA_CCP3_L	TMA_CCP3_H
0xA8	IE	P0_ID	TMA_PWM_CTRL2	TMA_PWM_CTRL3	TMA_PWM_OVRD	TMA_PWM_DTIME	TMA_CCP0_L	TMA_CCP0_H

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xA0	P2	P2_ID	TMA_CAP_CTRL1		TMA_CAP_INTEN	TMA_CAP_INTSTS	TMA_PWM_CTRL0	TMA_PWM_CTRL1
0x98	SCON0	SBUF0	TMA_CTRL	TMA_PLOAD_L	TMA_PLOAD_H	TMA_L	TMA_H	TMA_CAP_CTRL0
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Table 5-7 SFR memory map

PAGE_SW			Common / Address: 0x97		Page Switch Register			
Bit	7	6	5	4	3	2	1	0
Function	STORE_RESTORE		STORE_ERR	PAGE_SP		--	PAGE_NUM	
Default	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>STORE_RESTORE</td><td>W</td><td>PAGE_NUM load or restore contorl bit.
<table>
<tr><td>STORE_RESTORE</td><td>Description</td></tr>
<tr><td>0X</td><td>The PAGE_NUM is directly updated by CPU write and PAGE_SP is inactive.</td></tr>
<tr><td>10</td><td>The latest page number is written to the PAGE_NUM. In the same time, the previous contents of PAGE_NUM are saved in the storage register which is indicated by PAGE_SP.</td></tr>
<tr><td>11</td><td>The PAGE_NUM is overwritten by the contents of the storage register which indicated by PAGE_SP and the CPU write will be ignored.</td></tr>
</table></td><td></td></tr>
<tr><td>5</td><td>STORE_ERR</td><td>R/W</td><td>This bit is used to indicate the status of PAGE_NUM store / restore function.
read:
0: page number store / restore function is normally operating.
1: page number store / restore function is abnormally. Because successive store or restore is over 2 times.
write:
0: clears this bit
1: no effect</td><td></td></tr>
<tr><td>4:3</td><td>PAGE_SP</td><td>R</td><td>Page number storage pointer</td><td></td></tr>
<tr><td>2</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>1:0</td><td>PAGE_NUM</td><td>R/W</td><td>These bits indicate which SFR page is active now.
00: page 0
01: page 1
10: page 2
11: page 3</td><td></td></tr>
</table>

Table 5-8 The PAGE_SW register

5.2.4. Memory Related SFR

The following sub-sections describe program, external and internal memories related SFRs of 8051 core and their functionality. For other information about standard SFRs, please refer to appropriate peripheral section.

5.2.4.1. Program write enable bit

The Program Write Enable (PWE) bit, located in PCON register bit 4, is used during MOVX instructions. When PWE bit is set to "1", the MOVX @DPTR, an instruction writes data located in accumulator register into program memory addressed by DPTR register. Program memory can be read by MOVC only regardless of PWE bit.

5.2.4.2. Data pointer registers

Dual data pointer registers are implemented to speed up data block copying. DPTR0 and DPTR1 are located in four SFR addresses. Active DPTR register is selected by SEL bit (DPS[0]). If SEL=0, DPTR0 is selected, otherwise DPTR1.

5.2.4.3. Stack pointer

The CPU 8051 has 8-bit stack pointer called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET, and RETI execution. In the other words, it always points to the last valid stack byte. The SP is accessed as any other SFRs. **Figure 5-3** shows an example when PUSH A is executed and Figure 5-4 shows an example when POP PSW is executed.

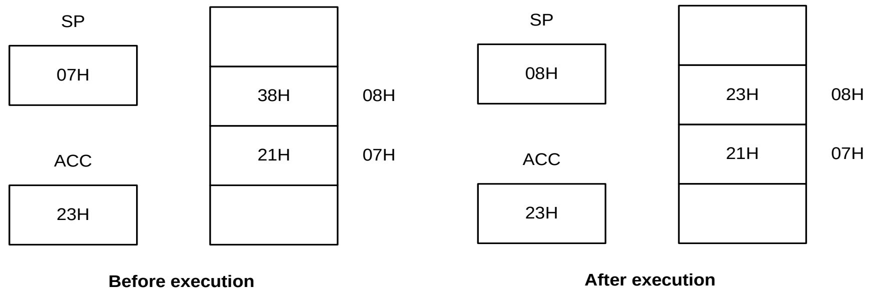


Figure 5-3 Stack byte order for PUSH A instruction

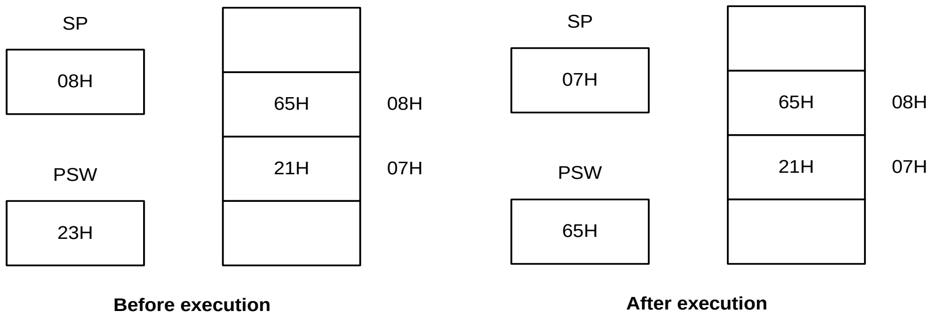


Figure 5-4 Stack byte order for POP PSW instruction

PCON			Common / Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 double baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: FLASH write activity during MOVX instruction disabled 1: FLASH write activity during MOVX instruction enabled	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-9 The PCON register

DPH0			Common / Address: 0x83		Data Pointer Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[15:8]	R/W	Data pointer register DPTR0 - high byte	

Table 5-10 The DPH0 register

DPL0			Common / Address: 0x82		Data Pointer Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[7:0]	R/W	Data pointer register DPTR0 - low byte	

Table 5-11 The DPL0 register

DPH1			Common / Address: 0x85		Data Pointer 1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[15:8]	R/W	Data pointer 1 register DPTR1 - high byte	

Table 5-12 The DPH1 register

DPL1			Common / Address: 0x84		Data Pointer 1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[7:0]	R/W	Data pointer 1 register DPTR1 - low byte	

Table 5-13 The DPL1 register

DPS			Common / Address: 0x86		Data Pointer Select Register			
Bit	7	6	5	4	3	2	1	0
Function	ID1	ID0	TSL	-	-	-	-	SEL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	ID[1:0]	R/W	Increment/decrement function selection. See Table **5-15**	
5	TSL	R/W	Toggle selection enable bit 0: DPTR related instructions do not affect state of SEL bit 1: DPTR related instructions to toggle the SEL bit Note: The DPTR related instructions are as below a. MOVX A,@DPTR b. MOVX @DPTR,A c. INC DPTR d. MOV DPTR,#data16 e. MOVC A,@A+DPTR	
4:1	--	R/W	Reserved	
0	SEL	R/W	Active data pointer selection bit See Table **5-15**	

Table 5-14 The DPS register

ID1	ID0	SEL=0	SEL=1
0	0	INC DPTR0	INC DPTR1
0	1	DEC DPTR0	INC DPTR1
1	0	INC DPTR0	DEC DPTR1
1	1	DEC DPTR0	DEC DPTR1

Table 5-15 DPTR0/DPTR1 operations

SP			Common / Address: 0x81		Stack Pointer Register			
Bit	7	6	5	4	3	2	1	0
Function	SP[7:0]							
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:0	SP[7:0]	R/W	Stack pointer	

Table 5-16 SP register

5.3. Special Function Registers (SFR)

GPM8F3331B has up to 187 control registers for special function registers. All SFRs are used by MCU and peripheral function block for controlling the desired operation. Some of the SFRs contain control and status bits for peripheral module such as Timer unit, Interrupt control unit, etc. Some bits in SFRs are read only, and so that writing to those bits don't have any effect on corresponding bits. Some SFRs have key code design that KEYCODE register must be written with correct key codes in sequence before writing a value to it for software safe. The following table shows the summary of the SFRs. The detailed information of each SFR is explained in each section.

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
Any	0x80	P0		0xFF	Port 0							
Any	0x81	SP		0x07	Stack Pointer							
Any	0x82	DPL0		0x00	Data pointer register DPTR0 - low byte							
Any	0x83	DPH0		0x00	Data pointer register DPTR0 - high byte							
Any	0x84	DPL1		0x00	Data pointer register DPTR1 - low byte							
Any	0x85	DPH1		0x00	Data pointer register DPTR1 - high byte							
Any	0x86	DPS		0x00	ID1	ID0	TSL	--	--	--	--	SEL
Any	0x87	PCON		0x00	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Any	0x88	TCON		0x00	TF1	TR1	TF0	TR0	ADC_INTF	--	TA_INTF	--
Any	0x89	TMOD		0x00	--	CT1	M11	M10	--	CT0	M01	M00
Any	0x8A	TL0		0x00	Timer 0 Load value – low byte							
Any	0x8B	TL1		0x00	Timer 1 Load value – low byte							
Any	0x8C	TH0		0x00	Timer 0 Load value – high byte							
Any	0x8D	TH1		0x00	Timer 1 Load value – high byte							
Any	0x8E	CKCON		0x07	WD1	WD0	WDFM	T1M	T0M	--	--	--
Any	0x90	P1		0xFF	Port 1							
Any	0x91	EIF		0x00	--	--	--	EXTF	LVDF	SPIF	I2CF	--
Any	0x97	PAGE_SW		0x00	STORE_RESTORE[1:0]		STORE_ER R	PAGE_SP[1:0]		--	PAGE_NUM[1:0]	
Any	0x98	SCON0		0x00	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Any	0x99	SBUF0		N/A	UART 0 buffer							
Any	0xA0	P2		0xFF	Port 2							
Any	0xA1	P2_ID		0xXX	Port 2 input data							
Any	0xA8	IE		0x00	EA	ETC	ETB	ES0	ET1	EADC	ET0	ETA
Any	0xA9	P0_ID		0xXX	Port 0 input data							
Any	0xB0	P3		0xFF	--	--	--	Port 3[4:0]				
Any	0xB1	P3_ID		0xXX	--	--	--	Port 3 input data[4:0]				
Any	0xB8	IP		0x00	--	PTC	PTB	PS0	PT1	PADC	PT0	PTA
Any	0xB9	P1_ID		0xXX	Port 1 input data							
Any	0xD0	PSW		0x00	CY	AC	F0	RS1	RS0	OV	F1	P
Any	0xD8	WDCON	AA/55	0x00	--	--	--	EWDI	WDIF	--	EWT	RWT
Any	0xE0	ACC		0x00	ACC register							
Any	0xE7	EXT_INT _FLAG		0x00	--	--					EXT_INT_FLAG[1:0]	
Any	0xE8	EIE		0x00	--	--	EWD	EEXT	ELVD	ESPI	EI2C	--
Any	0xEB	KEYCODE		0x00	Key Code							
Any	0xEC	FLH_CTRL0	8F/32/51	0xF8	--	--	--	--	--	--	FLH_PERA SE	FLH_PROG

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
Any	0xED	FLH_CTRL1	8F/32/51	0xE0	--	--	--	FLASH_LEVEL[4:0]				
Any	0xF0	B		0x00	B register							
Any	0xF8	EIP		0x00	--	--	PWDI	PEXT	PLVD	PSPI	PI2C	--
Any	0xFE	SYS_CTRL5	8F/32/50	0xFF	TMR_CKEN	OP_CMP_CKEN	--	--	SPI_CKEN	UART_CKEN	I2C_CKEN	ADC_CKEN
Any	0xFF	SYS_CTRL6	8F/32/50	0x00	UART_IF_SEL[1:0]		UART_IF_EN	T01_CK_SEL	--	AERR_RST EN	WDOG_CK EN	--

Table 5-17 The common SFR register

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0	0x9E	BODY_ID0		N/A	BODY ID0							
0	0x9F	BODY_ID1		N/A	BODY ID1							
0	0xA2	P2_DIR		0x00	Port 2 direction control bit							
0	0xA3	P2_ATT		0x00	Port 2 attribute control bit							
0	0xA4	P2_DS		0x00	Port 2 driving capability control bit							
0	0xA5	P2_SR		0x00	Port 2 slew rate control bit							
0	0xA6	P2_SMT		0x00	Port 2 Schmitt trigger control bit							
0	0xAA	P0_DIR		0x00	Port 0 direction control bit							
0	0xAB	P0_ATT		0x00	Port 0 attribute control bit							
0	0xAC	P0_DRV		0x00	Port 0 driving capability control bit							
0	0xAD	P0_SR		0x00	Port 0 slew rate control bit							
0	0xAE	P0_SMT		0x00	P0 Schmitt trigger control bit							
0	0xB2	P3_DIR		0x00	--	--	--	Port 3 direction control bit[4:0]				
0	0xB3	P3_ATT		0x00	--	--	--	Port 3 attribute control bit[4:0]				
0	0xB4	P3_DS		0x00	--	--	--	Port 3 driving capability control bit[4:0]				
0	0xB5	P3_SR		0x00	--	--	--	Port 3 slew rate control bit[4:0]				
0	0xB6	P3_SMT		0x00	--	--	--	Port 3 Schmitt trigger control bit[4:0]				
0	0xBA	P1_DIR		0x00	Port 1 direction control bit							
0	0xBB	P1_ATT		0x00	Port 1 attribute control bit							
0	0xBC	P1_DS		0x00	Port 1 driving capability control bit							
0	0xBD	P1_SR		0x00	Port 1 slew rate control bit							
0	0xBE	P1_SMT		0x00	P1 Schmitt trigger control bit							
0	0xD9	I2C_CTRL0		0x00	MST_STR	MST_STP	MST_NACK	I2C_MODE	I2C_CLK_SEL[1:0]		I2C_TRIG	I2C_EN
0	0xDA	I2C_CTRL1		0x08	--	--	--	--	SCL_STH_EN	ADR_MODE	ERR_SADR_IE	I2C_INTE
0	0xDB	I2C_DBT		0x00	--		I2C_DB_TIME[5:0]					
0	0xDC	I2C_STS0		0x40	RX_NEMP	TX_EMP	ARB_LOST	SLV_ADR_OK	SLV_DAT OK	SLV_STP_OK	NO_ACK	TRS_DONE
0	0xDD	I2C_STS1		0x00	--	--	--	URUN	ORUN	SLV_ADR_ERR	BUSY	GEN_CALL
0	0xE1	I2C_ADDR1		0x00	I2C_ADDR1[6:0]							R_W
0	0xE2	I2C_ADDR2		0x00	I2C_ADDR2[7:0]							
0	0xE3	I2C_TXDATA		0x00	I2C_TX_DATA[7:0]							
0	0xE4	I2C_RXDATA		0x00	I2C_RX_DATA[7:0]							

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0	0xE5	EXT_INT_EN		0x00	DEBOUNCE_TIME[1:0]		--	--	--	--	EXT_INT_EN[1:0]	
0	0xE6	EXT_INT_EDGE		0x00	--	--	--	--	--	--	EXT_INT_EDGE[1:0]	
0	0xF9	SYS_CTRL0	8F/32/50	0x00	--	CLK_DIV[1:0]		--	--	X8M_STABLE	MISS_X8MCLK	XTAL_EN
0	0xFA	SYS_CTRL1	8F/32/50	0x00	PLL_LOCKIN	PLL_N[1:0]		CLK_DIV_SEL	XTAL_IOSC_SEL	CLK_SRC_SEL	PLL_CHG_EN	PLL_EN
0	0xFB	SYS_CTRL2	8F/32/50	0x08	--	--	--	LDO33_EN	V15_SEL[1:0]		--	--
0	0xFC	SYS_CTRL3	8F/32/50	0x01	SW_RST_EN	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
0	0xFD	SYS_CTRL4	8F/32/50	0x00	POR_RST	WDOG_RST	--	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR

Table 5-18 The additional SFR register (page0)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
1	0x9A	ADC_CTRL0		0x00	ADC_OFSN[1:0]		ADC_OFSP[1:0]		ADC_VREF_SEL[2:0]			ADC_VREFE
1	0x9B	ADC_CTRL1		0x00	A_WDG_E	LOOP_E	DMA_EN	DMA_DB_EN		ADC_VREF_LOWCAP	ADC_EN	ADC_START
1	0x9C	ADC_CTRL2		0x00	--	ADC_CLK_SEL[2:0]				ADC_SH_SEL[2:0]		
1	0x9D	ADC_CTRL3		0x00	--	--	--	--	--	DMA_INTE	A_WDG_E	REG_INTE
1	0x9E	ADC_CTRL4		0x40	DMA_BUF_STATE	ADC_RDY	--	--	--	DMA_INTF	A_WDG_INTF	REG_INTF
1	0x9F	ADC_CTRL5		0x00	REG_SEQ_GAP			REG_CH_NUM				REG_E
1	0xA2	ADC_CTRL6		0x00	--	--	--	--	OFSET_CAL_TYP	ADC_OFSET_CAL_EN	ADC_D8B_EN	DATA_ALIGN
1	0xA3	ADC_REG_DATA_L		0x00	ADC_REG_DATA_Low Byte							
1	0xA4	ADC_REG_DATA_H		0x00	ADC_REG_DATA_High Byte							
1	0xA5	ADC_REG_SEQ0		0x00	REG_SEQ1				REG_SEQ0			
1	0xA6	ADC_REG_SEQ1		0x00	REG_SEQ3				REG_SEQ2			
1	0xA7	ADC_REG_SEQ2		0x00	REG_SEQ5				REG_SEQ4			
1	0xAA	ADC_REG_SEQ3		0x00	REG_SEQ7				REG_SEQ6			
1	0xAB	ADC_REG_SEQ4		0x00	REG_SEQ9				REG_SEQ8			
1	0xAC	ADC_REG_SEQ5		0x00	REG_SEQ11				REG_SEQ10			
1	0xAD	ADC_REG_SEQ6		0x00	REG_SEQ13				REG_SEQ12			
1	0xB2	ADC_WDG_		0x00	ADC_WDG_TH_HB_L							

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
		TH_HB_L										
1	0xB3	ADC_WDG_ TH_HB_H		0x00	--	--	--	--	ADC_WDG_TH_HB_H			
1	0xB4	ADC_WDG _TH_LB_L		0x00	ADC_WDG_TH_LB_L							
1	0xB5	ADC_WDG _TH_LB_H		0x00	--	--	--	--	ADC_WDG_TH_LB_H			
1	0xB6	ADC_WDG _SEL		0x00	--	--	--	--	ADC_WDG_CHSEL[3:0]			
1	0xBA	ADC_DMA_ TAR _ADDR_L		0x00	DMA_TAR_ADDR_L							
1	0xBB	ADC_DMA_ TAR_ADDR_H		0x00	DMA_TAR_ADDR_H							
1	0xBC	ADC_ OFSET_VAL		0x00	ADC_OFSET_VAL							
1	0xF1	OP_CTRL0		0x00	OP0_P _IF_EN	OP0_N _IF_EN	OP0_ CMP0_P	OP0_ CMP0_N	OP0_VREF_SEL[1:0]		Diode_EN	OP0_EN
1	0xF2	OP_CTRL1		0x00	OP1_P _IF_EN	OP1_CAP _IF_EN	OP1_O _IF_EN	OP1_ CMP1_P	OP1_ CMP1_N	OP1_PH _EN	OP1_GA _SEL	OP1_EN
1	0xF3	OP_CTRL2		0x00	OP2_N _IF_EN	--	OP2_ CMP1_P	OP2_ CMP1_N	OP2_VREF_SEL[1:0]		OP2_GA _SEL	OP2_EN
1	0xF5	CMP_CTRL0		0x00	CMP0_P _IF_EN	CMP0_N _IF_EN	CMP0_O	--	CMP0_HYS _SEL[1:0]		CMP0_HYS _EN	CMP0_EN
1	0xF6	CMP_CTRL1		0x00	CMP1_P _IF_EN	CMP1_N _IF_EN	CMP1_O	--	CMP1_HYS _SEL[1:0]		CMP1_HYS _EN	CMP1_EN
1	0xF7	CMP_CTRL2		0x00	CMP1_DEB _EN	--	CMP1_DEB _SEL[1:0]		CMP0_DEB _EN	--	CMP0_DEB _SEL[1:0]	
1	0xFD	Charge_ CTRL		0x00	--	--	--	VOL_P13		VOL_P12		IO33V_EN

Table 5-19 The additional SFR register (page1)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
2	0x9A	TMB_CTRL		0x00	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
2	0x9B	TMB_ PLOAD_L		0x00	Timer B pre-load data– low byte							
2	0x9C	TMB_ PLOAD_H		0x00	Timer B pre-load data – high byte							
2	0x9D	TMB_L		0x00	Timer B – low byte							
2	0x9E	TMB_H		0x00	Timer B – high byte							
2	0x9F	TMB_CAP_ CTRL0		0x00	--	--	--	--	--	--	TMB_CAP_EN[1:0]	
2	0xA2	TMB_CAP_ CTRL1		0x00					TMB_CAP1_EDGE[1:0]		TMB_CAP0_EDGE[1:0]	

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
2	0xA3	TMB_CAP_INTCTRL		0x00	--	--	TMB_CAP_STS[1:0]		--	--	TMB_CAP_INTEN[1:0]	
2	0xA4	TMB_PWM_CTRL0		0x00	--	--	--	TMB_PWM01_MODE	--	--	TMB_PWMx_EN[1:0]	
2	0xA5	TMB_PWM_CTRL1		0x00	PC1_PORT	PC0_PORT	--	DUTY_DIR_WR_EN	--	--	TMB_PWMx_POL[1:0]	
2	0xA6	TMB_PWM_DTIME		0x00	Timer B PWM dead time							
2	0xAA	TMB_CCP0_L		0x00	Timer B CCP0 – low byte							
2	0xAB	TMB_CCP0_H		0x00	Timer B CCP0 – high byte							
2	0xAC	TMB_CCP1_L		0x00	Timer B CCP1 – low byte							
2	0xAD	TMB_CCP1_H		0x00	Timer B CCP1 – high byte							
2	0xBA	TMC_CTRL		0x00	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
2	0xBB	TMC_PLOAD_L		0x00	Timer C pre-load data – low byte							
2	0xBC	TMC_PLOAD_H		0x00	Timer C pre-load data – high byte							
2	0xBD	TMC_L		0x00	Timer C – low byte							
2	0xBE	TMC_H		0x00	Timer C – high byte							
2	0xBF	TMC_CAP_CTRL0		0x00	--	--	--	--	Timer C capture enable[3:0]			
2	0xC2	TMC_CAP_CTRL1		0x00	TMC_CAP3_EDGE[1:0]		TMC_CAP2_EDGE[1:0]		TMC_CAP1_EDGE[1:0]		TMC_CAP0_EDGE[1:0]	
2	0xC4	TMC_CAP_INTEN		0x00	--	--	--	--	TMC_CAPx_INTEN[3:0]			
2	0xC5	TMC_CAP_INTSTS		0x00	--	--	--	--	TMC_CAPx_STS[3:0]			
2	0xC6	TMC_CAP0_L		0x00	TMC_CAP0 – low byte							
2	0xC7	TMC_CAP0_H		0x00	TMC_CAP0 – high byte							
2	0xCA	TMC_CAP1_L		0x00	TMC_CAP1 – low byte							
2	0xCB	TMC_CAP1_H		0x00	TMC_CAP1 – high byte							
2	0xCC	TMC_CAP2_L		0x00	TMC_CAP2 – low byte							
2	0xCD	TMC_CAP2_H		0x00	TMC_CAP2 – high byte							
2	0xCE	TMC_CAP3_L		0x00	TMC_CAP3 – low byte							
2	0xCF	TMC_CAP3_H		0x00	TMC_CAP3 – high byte							

Table 5-20 The additional SFR register (page2)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
3	0x9A	TMA_CTRL		0x00	TMA_EDGE	ALIGN_TYPE	TMA_INTF	TMA_INTEN	CLK_SRC_SEL[2:0]			TMA_EN
3	0x9B	TMA_PLOAD_L		0x00	Timer A pre-load data– low byte							
3	0x9C	TMA_PLOAD_H		0x00	Timer A pre-load data – high byte							
3	0x9D	TMA_L		0x00	Timer A – low byte							
3	0x9E	TMA_H		0x00	Timer A – high byte							
3	0x9F	TMA_CAP_CTRL0		0x00	--	--	--	--	Timer A capture enable[3:0]			
3	0xA2	TMA_CAP_CTRL1		0x00	TMA_CAP3_EDGE[1:0]		TMA_CAP2_EDGE[1:0]		TMA_CAP1_EDGE[1:0]		TMA_CAP0_EDGE[1:0]	
3	0xA4	TMA_CAP_INTEN		0x00	--	--	--	--	TMA_CAP_INTEN[3:0]			
3	0xA5	TMA_CAP_INTSTS		0x00	--	--	--	--	TMA_CAP_INTSTS[3:0]			
3	0xA6	TMA_PWM_CTRL0		0x00	DUTY_MODE	--	--	--	TMA_PWMx_EN[3:0]			
3	0xA7	TMA_PWM_CTRL1		0x00	OVC_EN	DUTY_DIR_WR_EN	--	--	--	TMA_PWM23_MODE	--	TMA_PWM01_MODE
3	0xAA	TMA_PWM_CTRL2		0x00	--		--	--	TMA_PWMx_POL[3:0]			
3	0xAB	TMA_PWM_CTRL3		0x0F	--	--	--	--	TMA_PWMx_CTR_SRC[3:0]			
3	0xAC	TMA_PWM_OVRD		0x00	--	--	--	--	TMA_PWMx_OVRD[3:0]			
3	0xAD	TMA_PWM_DTIME		0x00	Timer A PWM dead time							
3	0xAE	TMA_CCP0_L		0x00	Timer A CCP0 – low byte							
3	0xAF	TMA_CCP0_H		0x00	Timer A CCP0 – high byte							
3	0xB2	TMA_CCP1_L		0x00	Timer A CCP1 – low byte							
3	0xB3	TMA_CCP1_H		0x00	Timer A CCP1 – high byte							
3	0xB4	TMA_CCP2_L		0x00	Timer A CCP2 – low byte							
3	0xB5	TMA_CCP2_H		0x00	Timer A CCP2 – high byte							
3	0xB6	TMA_CCP3_L		0x00	Timer A CCP3 – low byte							
3	0xB7	TMA_CCP3_H		0x00	Timer A CCP3 – high byte							
3	0xC4	TMA_PWM0_END_L		0x00	Timer A PWM0 end edge – low byte							
3	0xC5	TMA_PWM0_END_H		0x00	Timer A PWM0 end edge – high byte							
3	0xC6	TMA_PWM1_END_L		0x00	Timer A PWM1 end edge – low byte							
3	0xC7	TMA_PWM1_END_H		0x00	Timer A PWM1 end edge – high byte							
3	0xCA	TMA_PWM2_		0x00	Timer A PWM2 end edge – low byte							

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
		END_L										
3	0xCB	TMA_PWM2_ END_H		0x00	Timer A PWM2 end edge – high byte							
3	0xCC	TMA_PWM3_ END_L		0x00	Timer A PWM3 end edge – low byte							
3	0xCD	TMA_PWM3_ END_H		0x00	Timer A PWM3 end edge – high byte							

Table 5-21 The additional SFR register (page3)

5.4. Clock Source

GPM8F3331B has three clock sources including internal oscillator (8MHz), external crystal (8MHz) and internal PLL clock source. These three clocks are chosen to be system clock source by controlling XTAL_IOSC_SEL, CLK_DIV_SEL and CLK_SRC_SEL bits of SYS_CTRL1 register. In addition, a clock divisor for the system clock source is contained to obtain different frequencies. There are totally four selections which can be controlled by CLK_DIV[1:0] bits of SYS_CTRL0 register. The block diagram of clock source and detailed description of SYS_CTRL0 and SYS_CTRL1 register are shown in **Figure 5-5**, **Table 5-22**, **Table 5-23**, **Table 5-24** and **Table 5-25** respectively.

The default system clock is 4MHz, which is by the IOSC8M divisor 2. If the clock source wants to use the XTAL8M, please setting the bit[0] of the SYS_CTRL0 and polling bit[2] of SYS_CTRL0 to assure this bit is be setting “1”. After X8M is stable, the third bit of SYS_CTRL1 can be set.

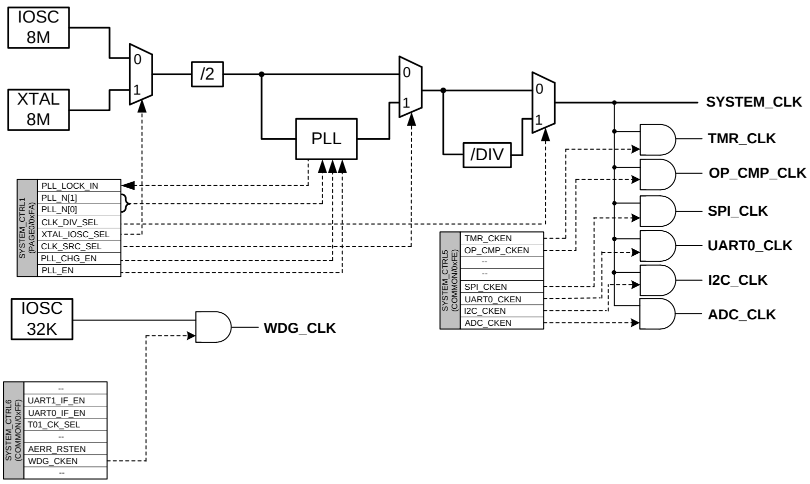


Figure 5-5 The block diagram of clock sources

SYS_CTRL0				**Page:0 / Address: 0xF9**		**System Control-0 Register**		
Bit	7	6	5	4	3	2	1	0
Function	--	CLK_DIV[1:0]		--	--	X8M_STABLE	MISS_X8M_CLK	XTAL_EN
Default	0	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7	--	--	Reserved	
6:5	CLK_DIV[1:0]	R/W	System Clock divider. This function will be disabled automatically if CLK_SRC_SEL[1] of SYS_CTRL1 register is set to 1. CLK_DIV: System Divider 00: Clock Source / 2 01: Clock Source / 4 10: Clock Source / 8 11: Clock Source / 16	
4	--	--	Reserved	
3	--	--	Reserved	
2	X8M_STABLE	R	XTAL_8M clock stable flag 0: Xtal_8m is not ready 1: Xtal_8m is ready	

Bit	Function	Type	Description	Condition
1	MISS_X8M_CLK	R	XTAL8M clock indicated flag 0: Xtal is in normal working 1: Missing xtal clock	
0	XTAL_EN	R/W	XTAL 8M PAD enable signal 0: Disabled 1: Enabled	

Table 5-22 SYS_CTRL0 register

SYS_CTRL1			Page:0 / Address: 0xFA		System Control-1 Register			
Bit	7	6	5	4	3	2	1	0
Function	PLL_LOCKIN	PLL_N[1:0]		CLK_DIV_SEL	XTAL_IOSC_SEL	CLK_SRC_SEL	PLL_CHG_EN	PLL_EN
Default	0	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7	PLL_LOCKIN	R	PLL lock-in flag 0: PLL is tracking or PLL is disabled. 1: PLL is locked-in	
6:5	PLL_N	R/W	PLL frequency select signals. PLL_N: PLL Output Frequency 00: 52.357MHz 01: 60.019MHz 10: 63.850MHz 11: 65.3824MHz	
4	CLK_DIV_SEL	R/W	System clock select signal 0: System clock = input clock source 1: System clock = input clock source / N	
3	XTAL_IOSC_SEL	R/W	XTAL8M or IOSC8M clock select signal 0: IOSC8M clock is system clock base 1: XTAL8M clock is system clock base	
2	CLK_SRC_SEL	R/W	Clock input source select signals. CLK_SRC_SEL: Clock Source 0: IOSC or XTAL clock / Div 2 1: PLL clock	
1	PLL_CHG_EN	R/W	PLL_N change enable signal. This bit must be set when users want to update PLL_N or 1st PLL enable. It will be cleared by hardware automatically. 0: Disabled 1: Enabled	
0	PLL_EN	R/W	Embedded PLL enable signal. 0: Disabled 1: Enabled	

Table 5-23 SYS_CTRL1 register

SYS_CTRL5			Common / Address: 0xFE		System Control-5 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMR _CKEN	OP_CMP _CKEN	--	--	SPI _CKEN	UART0 _CKEN	I2C _CKEN	ADC _CKEN
Default	1	1	1	1	1	1	1	1
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7	TMR _CKEN	R/W	Timer controller clock enable signal. 0: Disabled 1: Enabled	
6	OP_CMP_CKEN	R/W	OP and CMP controller clock enable signal 0: Disabled 1: Enabled	
5:4	--	R/W	Reserved	
3	SPI_CKEN	R/W	SPI controller clock enable signal. 0: Disabled 1: Enabled	
2	UART0_CKEN	R/W	UART0 controller clock enable signal. 0: Disabled 1: Enabled	
1	I2C_CKEN	R/W	I2C controller clock enable signal. 0: Disabled 1: Enabled	
0	ADC_CKEN	R/W	ADC controller clock enable signal. 0: Disabled 1: Enabled	

Table 5-24 SYS_CTRL5 register

SYS_CTRL6			Common / Address: 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL		UART_IF_EN	T01_CK_SEL	--	ADDR_RSTEN	WDOG_CKEN	--
Default	0	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7:6	UART_IF_SEL[1:0]	R/W	UART0 interface select 00: TX is P14 , RX is P15 (default) 01: TX is P24 , RX is P25 10: TX is P30 , RX is P31 11: Reserved	
5	UART_IF_EN	R/W	UART0 interface enable signal. 0: Disabled 1: Enabled	
4	T01_CK_SEL	R/W	Timer0/1 clock source selection signal. This bit is used for combining with T0M/T1M of CKCON(0x8E). T0M /T1M | T01_CK_SEL | Timer0/1 Clock	

Bit	Function	Type	Description			Condition
			0	0	System Clock / 8	
			0	1	System Clock / 2	
			1	0	System Clock / 4	
			1	1	System Clock / 1	
3	--	R/W	Reserved			
2	ADDR_RSTEN	R/W	FLASH address over range reset enable 0: Disabled 1: Enabled			
1	WDOG_CKEN	R/W	Watchdog controller clock enable control bit 0: Disabled 1: Enabled			
0	--	R/W	Reserved			

Table 5-25 SYS_CTRL6 register

5.5. Power Saving Mode

5.5.1. Introduction

Although GPM8F3331B is a high-speed microcontrollers designed for maximum performance, it also provides Power Management Unit (PMU) with an advanced power conservation modes. This mode is called "SLEEP mode". In order to reduce the current consumption when system does not need to be active, SLEEP mode can be utilized. For more information about this modes, please see the following section. **Table 5-26** shows the two operating modes in GPM8F3331B. In addition, user can save power consumption by reducing core power voltage via setting SYS_CTRL2.V15_SEL.

5.5.2. SLEEP mode

SLEEP mode is the lowest power consumption state the microcontroller can enter. It is achieved by cutting-off frequency provided to system clock, resulting in a fully static condition. Processor operation will be postponed on the instruction that sets the STOP bit. SLEEP mode can withdraw by an non-system-clocked interrupt such as the watchdog interrupt, external interrupts EXT_IRQ0 and EXT_IRQ1. After wakeup source trigger, processor operation will resume with the fetching of the interrupt vector associated with the interrupt that caused the exit from SLEEP mode. When the interrupt service routine is completed, RETI returns the program to the instruction immediately following the one that invoked the SLEEP mode. When EXT_IRQ0 and EXT_IRQ1 are used for wakeup source, EXT_INT_EN and EXT_INT_EDGE register must be set as shown in **Table 5-28** and **Table 5-29**. The SLEEP mode operation flowed is showmen as **Figure 5-6** .

In order to reduce power consumption when system operating in normal mode. User can switch-off clock of unused block by individual register setting. These register descriptions are shown as **Table 5-33** and **Table 5-34**.

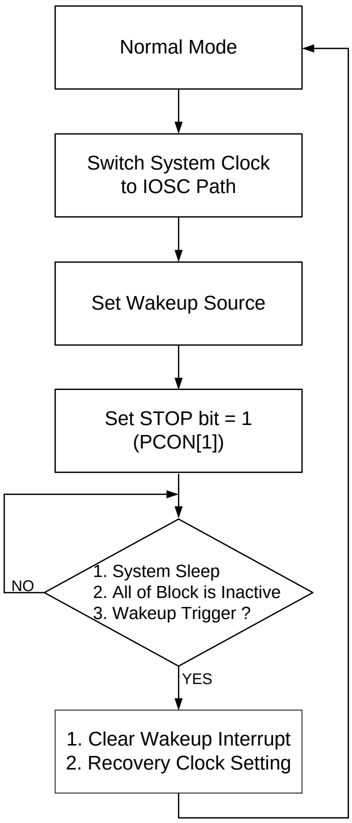


Figure 5-6 The SLEEP mode operating flow

	CPU clock	Peripheral clock	Wakeup source	After wakeup
Normal Mode	ON	Register setting	--	--
SLEEP Mode	OFF	OFF	1. External Interrupt 2. WDG Interrupt	Next instruction state

Table 5-26 Two operation modes in GPM8F3331B

PCON			Common / Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 double baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: Disables FLASH write activity during MOVX instruction 1: Enables FLASH write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-27 The PCON register

EXT_INT_EN			Page: 0 / Address: 0xE5		External Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	DEBOUNCE_TIME[1:0]		--	--	--	--	EXT_INT1_EN	EXT_INT0_EN
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	DEBOUNCE_TIME	R/W	External interrupt de-bounce time select signal DEBOUNCE_TIME[1:0] : Clock Cycle 00 : 4 01 : 37 10 : 72 11 : 142	
5:2	--	R/W	Reserved	
1	EXT_INT1_EN	R/W	External interrupt 1 enable signal that is mapped to P1_5. 0: disabled 1: enabled	
0	EXT_INT0_EN	R/W	External interrupt 0 enable signal that is mapped to P1_4. 0: disabled 1: enabled	

Table 5-28 The EXT_INT_EN register

EXT_INT_EDGE			Page: 0 / Address: 0xE6		External Interrupt Edge Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	EXT_INT1_EDGE	EXT_INT0_EDGE
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	EXT_INT1_EDGE	R/W	External interrupt 1 trigger edge control signal 0: Falling edge 1: Rising edge	
0	EXT_INT0_EDGE	R/W	External interrupt 0 trigger edge control signal 0: Falling edge 1: Rising edge	

Table 5-29 The EXT_INT_EDGE register

EXT_INT_FLAG			Common / Address: 0xE7		External Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	EXT_INT1 _FLAG	EXT_INT0 _FLAG
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	EXT_INT1_FLAG	R/W	External interrupt 1 flag read: 0: External interrupt is not occurred 1: External interrupt is occurred write: 0: Clears this bit 1: No effect	
0	EXT_INT0_FLAG	R/W	External interrupt 0 flag read: 0: External interrupt is not occurred 1: External interrupt is occurred write: 0: Clears this bit 1: No effect	

Table 5-30 The EXT_INT_FLAG register

WDCON			Common / Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	EWDI	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0
keycode	AA/55							

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
4	EWDI	R/W	Enable Watchdog interrupt 0: Disabled 1: Enabled	

Bit	Function	Type	Description	Condition
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disabled; 1: Enabled	
0	RWT	R/W	Reset watchdog timer 0: NA; 1: Reset	

Table 5-31 WDCON register

CKCON			Common / Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>WD[1:0]</td><td>R/W</td><td>Watchdog timeout selection bits
If WDFM=0:
<table>
<tr><td>WD[1:0]</td><td>Timeout</td></tr>
<tr><td>00</td><td>16ms</td></tr>
<tr><td>01</td><td>64ms</td></tr>
<tr><td>10</td><td>256ms</td></tr>
<tr><td>11</td><td>1024ms</td></tr>
</table>
If WDFM=1:
<table>
<tr><td>WD[1:0]</td><td>Timeout</td></tr>
<tr><td>00</td><td>1ms</td></tr>
<tr><td>01</td><td>2ms</td></tr>
<tr><td>10</td><td>4ms</td></tr>
<tr><td>11</td><td>8ms</td></tr>
</table></td><td></td></tr>
<tr><td>5</td><td>WDFM</td><td>R/W</td><td>Watchdog fast mode selection bit
0: Watchdog fast mode is disabled
1: Watchdog fast mode is enabled</td><td></td></tr>
<tr><td>4</td><td>T1M</td><td>R/W</td><td>Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table>
<tr><td>T1M</td><td>T01_CK_SEL</td><td>Timer1 Clock</td></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>3</td><td>T0M</td><td>R/W</td><td>Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table>
<tr><td>T0M</td><td>T01_CK_SEL</td><td>Timer0 Clock</td></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
</table></td><td></td></tr>
</table>

Bit	Function	Type	Description			Condition
			1	1	System Clock / 1	
2:0	--	R/W	Reserved			

Table 5-32 CKCON register

SYS_CTRL5			Common / Address: 0xFE		System Control-5 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMR _CKEN	OP_CMP _CKEN	--	--	SPI _CKEN	UART0 _CKEN	I2C _CKEN	ADC _CKEN
Default	1	1	1	1	1	1	1	1
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7	TMR _CKEN	R/W	Timer controller clock enable signal 0: Disabled 1: Enabled	
6	OP_CMP_CKEN	R/W	OP and CMP controller clock enable signal 0: Disabled 1: Enabled	
5:4	--	R/W	Reserved	
3	SPI_CKEN	R/W	SPI controller clock enable signal 0: Disabled 1: Enabled	
2	UART0_CKEN	R/W	UART0 controller clock enable signal 0: Disabled 1: Enabled	
1	I2C_CKEN	R/W	I2C controller clock enable signal 0: Disabled 1: Enabled	
0	ADC_CKEN	R/W	ADC controller clock enable signal 0: Disabled 1: Enabled	

Table 5-33 SYS_CTRL5 register

SYS_CTRL6			Common / Address: 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL		UART_IF_EN	T01_CK_SEL	--	ADDR_RSTEN	WDOG_CKEN	--
Default	0	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7:6	UART_IF_SEL[1:0]	R/W	UART0 interface selection 00: TX is P14; RX is P15 (default) 01: TX is P24; RX is P25 10: TX is P30; RX is P31 11: Reserved	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>5</td><td>UART_IF_EN</td><td>R/W</td><td>UART0 interface enable signal.
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>4</td><td>T01_CK_SEL</td><td>R/W</td><td>Timer0/1 clock source select signal. This bit is used combining with T0M/T1M of CKCON(0x8E).
<table>
<tr><th>T0M /T1M</th><th>T01_CK_SEL</th><th>Timer0/1 Clock</th></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>3</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>2</td><td>ADDR_RSTEN</td><td>R/W</td><td>FLASH address over range reset enable
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>1</td><td>WDOG_CKEN</td><td>R/W</td><td>Watchdog controller clock enable control bit
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-34 SYS_CTRL6 register

<table>
<tr><th colspan="3">SYS_CTRL2</th><th colspan="2">Page:0 / Address: 0xFB</th><th colspan="4">System Control-2 Register</th></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Function</td><td>--</td><td>--</td><td>--</td><td>LDO33_EN</td><td colspan="2">V15_SEL[1:0]</td><td>--</td><td>--</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Key Code</td><td colspan="8">0x8F / 0x32 / 0x50</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:5</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>4</td><td>LDO33_EN</td><td>R/W</td><td>3.3V power enable
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>3:2</td><td>V15_SEL</td><td>R/W</td><td>1.5V power domain selection bit.
<table>
<tr><th>V15_SEL[1:0]</th><th>Voltage of V15</th></tr>
<tr><td>00</td><td>1.6V</td></tr>
<tr><td>01</td><td>prohibit</td></tr>
<tr><td>10</td><td>1.65V</td></tr>
<tr><td>11</td><td>1.7V</td></tr>
</table></td><td></td></tr>
<tr><td>1</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-35 SYS_CTRL2 register

5.6. Interrupt System

5.6.1. Introduction

The GPM8F3331B provides 11 types of interrupt sources with 2-level interrupt priority control, see **Table 5-36**. For standard 8051 interrupt sources, each interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8) and EIP(0xF8) registers. INT0 has the top priority in default state and user can choose the related interrupt source to be the top priority by IP register. Interrupt requests are sampled each system clock at the rising edge of clock control. Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), EIE(0xE8). The IE contains global interrupt system disable(0) / enable(1) bit called EA.

In general, once an interrupt event occurs, the corresponding flag bit will be set. The related registers of interrupt flag are described as below.

If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and then CPU will execute service routine. If the related interrupt control bit is disabled, programmer can still observe the corresponding flag bit, but no interrupt request signal will be generated. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock in interrupt service routine. With any instruction, interrupts pending during the previous instruction is served. Before entering interrupt service routine, system saves the current PC address into top of stack and jumps to corresponding vector to execute the interrupt service. After finishing the interrupt service, the system abstracts the returned PC address from the top of the stack to execute the following instruction.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Vector number	Priority
TAF	Timer A Interrupt	--	Software(cleared by 0)	0x03	0	1
T0F	Timer 0 Interrupt	--	Hardware	0x0B	1	2
ADCF	ADC Interrupt	--	Software(cleared by 0)	0x13	2	3
T1F	Timer 1 Interrupt	--	Hardware	0x1B	3	4
TI0 & RI0	UART0 Interrupt	--	Software(cleared by 0)	0x23	4	5
TBF	Timer B Interrupt	--	Software(cleared by 0)	0x2B	5	6
TCF	Timer C Interrupt	--	Software(cleared by 0)	0x33	6	7
--	--	--	Software(cleared by 0)	0x3B	7	8
I2CF	I2C Interrupt	--	Software(cleared by 0)	0x43	8	9
SPIF	SPI Interrupt	--	Software(cleared by 0)	0x4B	9	10
LVDF	LVD	--	Software(cleared by 0)	0x53	10	11
EXTF	External Interrupt	Rising/Falling	Software(cleared by 0)	0x5B	11	12
WDIF	Watchdog Interrupt	--	Software(cleared by 0)	0x63	12	13

Table 5-36 Summaries of all interrupt sources

IP			Common /Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	-	PTC	PTB	PS0	PT1	PADC	PT0	PTA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	PTC	R/W	Timer C interrupt priority level control (1: high level)	
5	PTB	R/W	Timer B interrupt priority level control (1: high level)	
4	PS0	R/W	UART0 interrupt priority level control (1: high level)	
3	PT1	R/W	Timer 1 interrupt priority level control (1: high level)	
2	PADC	R/W	ADC0/1 interrupt priority level control (1: high level)	
1	PT0	R/W	Timer 0 interrupt priority level control (1: high level)	
0	PTA	R/W	Timer A interrupt priority level control (1: high level)	

Table 5-37 IP register

EIP			Common / Address: 0xF8		Extended Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	PWDI	PEXT	PLVD	PSPI	PI2C	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	PWDI	R/W	Watchdog interrupt priority level control (1: high level)	
4	PEXT	R/W	External interrupt priority level control (1: high level)	
3	PLVD	R/W	LVD interrupt priority level control (1: high level)	
2	PSPI	R/W	SPI interrupt priority level control (1: high level)	
1	PI2C	R/W	I2C interrupt priority level control (1: high level)	
0	--	R/W	Reserved	

Table 5-38 EIP register

IE			Common /Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	ETC	ETB	ES0	ET1	EADC	ET0	ETA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enables global interrupts	
6	ETC	R/W	Enables Timer C interrupt	
5	ETB	R/W	Enables Timer B interrupt	
4	ES0	R/W	Enables UART0 interrupt	
3	ET1	R/W	Enables Timer 1 interrupt	
2	EADC	R/W	Enables ADC interrupt	
1	ET0	R/W	Enables Timer 0 interrupt	
0	ETA	R/W	Enables Timer A interrupt	

Table 5-39 IE register

EIE			Common /Address: 0xE8		Extended Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	-	-	EWD	EEXT	ELVD	ESPI	EI2C	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	EWD	R/W	Enables watchdog interrupt	
4	EEXT	R/W	Enables External interrupts	
3	ELVD	R/W	Enables LVD interrupts	
2	--	R/W	Reserved	
1	EI2C	R/W	Enables I2C interrupts	

Bit	Function	Type	Description	Condition
0	--	R/W	Reserved	

Table 5-40 EIE register

TCON			Common /Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	ADC_INTF	--	TA_INTF	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: Disabled 1: Enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: Disabled 1: Enabled	
3	ADC_INTF	R	ADC interrupt flag	
2	--	R/W	Reserved	
1	TA_INTF	R	Timer A interrupt flag	
0	--	R/W	Reserved	

Table 5-41 TCON register

WDCON			Common/Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	EWDI	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0
keycode	AA/55							

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	EWDI	R/W	Enable Watchdog interrupt 0: Disabled 1: Enabled	
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disabled; 1: Enabled	
0	RWT	R/W	Reset watchdog timer 0: NA; 1: Reset	

Table 5-42 WDCON register

SCON0			Common/Address: 0x98		UART0 configuration register			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting which described as Table 5-172	
5	SM02	R/W	Enable a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0, this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received.	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-43 SCON0 register

EIF			Common/Address: 0x91		Extended interrupt flag			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	EXTF	LVDF	SPIF	I2CF	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	EXTF	R/W	External interrupt flag	
3	LVDF	R/W	LVD interrupt flag	
2	--	R/W	Reserved	
1	I2CF	R/W	I2C interrupt flag	
0	--	R/W	Reserved	

Table 5-44 EIF register

TMA_CTRL			Page: 3 / Address: 0x9A		Timer A Control Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_EDGE	ALIGN_TYPE	TMA_INTF	TMA_INTEN	CLK_SRC_SEL			TMA_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMA_EDGE	R	Timer A up/down count edge indication flag. 0: Falling edge 1: Rising edge	
6	ALIGN_TYPE	R/W	0: Edge alignment 1: Center alignment	
5	TMA_INTF	R/W	Timer A interrupt flag read : 0: Idle / busy 1: Timer A interrupt trigger	

Bit	Function	Type	Description	Condition
			write : 0: Clears this bit 1: No effect	
4	TMA_INTEN	R/W	Timer A interrupt enable signal 0: Disabled 1: Enabled	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer A input clock source select signal. CLK_SRC_SEL[2:0] = Clock Source: 000 = System clock 001 = System clock / 2 010 = System clock / 4 011 = System clock / 8 100 = System clock / 16 101 = System clock / 32 110 = IOSC_8M 111 = 32K (IOSC_32K) Note: when CLK_SRC_SEL select IOSC8M , the system clock must faster more 2 times than IOSC8M.	
0	TMA_EN	R/W	Timer A enable signal. 0: Disabled 1: Enabled	

Table 5-45 TMA_CTRL register

TMA_CAP_INTEN			Page: 3 / Address: 0xA4		Timer A Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_CAPx_INTEN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMA_CAPx_INTEN[3:0]	R/W	Timer A capture mode interrupt enable control bits. These are mapped to CAP0 ~ CAP3 respectively. 0: Disabled 1: Enabled	

Table 5-46 TMA_CAP_INTEN register

TMA_CAP_INTSTS			Page: 3 / Address: 0xA5		Timer A Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_CAPx_INTSTS[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMA_CAPx_INTSTS[3:0]	R/W	Timer A capture mode interrupt status register. These are mapped to CAP0 ~ CAP3 respectively.	

Bit	Function	Type	Description	Condition
			read: 0: No capture triggered 1: Capture triggered write: 0: Clears this bit 1: No effect	

Table 5-47 TMA_CAP_INTSTS register

TMB_CTRL			**Page: 2 / Address: 0x9A**		**Timer B Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
Default	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7</td><td>TMB_EDGE</td><td>R</td><td>Timer B up/down count edge indication flag.
0: Falling edge
1: Rising edge</td><td></td></tr>
<tr><td>6</td><td>ALIGN_TYPE</td><td>R/W</td><td>0: Edge alignment
1: Center alignment</td><td></td></tr>
<tr><td>5</td><td>TMB_INTF</td><td>R/W</td><td>Timer B interrupt flag
read :
0: Idle / busy
1: Timer B interrupt trigger
write :
0: Clears this bit
1: No effect</td><td></td></tr>
<tr><td>4</td><td>TMB_INTEN</td><td>R/W</td><td>Timer B interrupt enable signal
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>3:1</td><td>CLK_SRC_SEL[2:0]</td><td>R/W</td><td>Timer B input clock source select signal.
<table>
<tr><td>CLK_SRC_SEL[2:0]</td><td>Clock Source</td></tr>
<tr><td>000</td><td>System clock</td></tr>
<tr><td>001</td><td>System clock / 2</td></tr>
<tr><td>010</td><td>System clock / 4</td></tr>
<tr><td>011</td><td>System clock / 8</td></tr>
<tr><td>100</td><td>System clock / 16</td></tr>
<tr><td>101</td><td>System clock / 32</td></tr>
<tr><td>110</td><td>IOSC_8M</td></tr>
<tr><td>111</td><td>32K (IOSC_32K)</td></tr>
</table>
Note: when CLK_SRC_SEL select IOSC8M , the system clock must faster more 2 times than IOSC8M.</td><td></td></tr>
<tr><td>0</td><td>TMB_EN</td><td>R/W</td><td>Timer B enable signal.
0: Disabled
1: Enabled</td><td></td></tr>
</table>

Table 5-48 TMB_CTRL register

TMB_CAP_INTCTRL			Page: 2 / Address: 0xA3		Timer B Capture Mode Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMB_CAP_INTSTS[1:0]		--	--	TMB_CAP_INTEN[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:4	TMB_CAP_INTSTS[1:0]	R/W	Timer B capture mode trigger flag. These are mapped to CAP0 ~ CAP1 respectively. read: 0: No capture signal triggered 1: Capture signal triggered write: 0: Clears this bit 1: No effect	
3:2	--	R/W	Reserved	
1:0	TMB_CAP_INTEN[1:0]	R/W	Timer B capture mode interrupt enable control bits. These are mapped to CAP0 ~ CAP1 respectively. 0: Disabled 1: Enabled	

Table 5-49 TMB_CAP_INTCTRL registers

TMC_CTRL			Page: 2 / Address: 0xBA		Timer C Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	TMC_INTF	R/W	Timer C interrupt flag read: 0: Idle / busy 1: Timer C interrupt trigger write: 0: Clears this bit 1: No effect	
4	TMC_INTEN	R/W	Timer C interrupt enable signal 0: Disabled 1: Enabled	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer C input clock source select signal. CLK_SRC_SEL[2:0] → Clock Source: 000: System clock 001: System clock / 2 010: System clock / 4 011: System clock / 128 100: System clock / 256	

Bit	Function	Type	Description		Condition
			101	System clock / 512	
			110	System clock / 1024	
			111	Prohibit	
0	TMC_EN	R/W	Timer C enable signal 0: Disabled 1: Enabled		

Table 5-50 TMC_CTRL register

TMC_CAP_INTEN			Page: 2 / Address: 0xC4		Timer C Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMC_CAPx_INTEN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMC_CAPx_INTEN[3:0]	R/W	Timer C capture mode interrupt enable control bits. These are mapped to CAP0 ~ CAP3 respectively. 0: Disabled 1: Enabled	

Table 5-51 TMC_CAP_INTEN register

TMC_CAP_INTSTS			Page: 2 / Address: 0xC5		Timer C Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMC_CAPx_INTSTS[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	TMC_CAPx_INTSTS[3:0]	R/W	Timer C capture mode interrupt status register. These are mapped to CAP0 ~ CAP3 respectively. read : 0: No capture triggered 1: Capture triggered write : 0: Clears this bit 1: No effect	

Table 5-52 TMC_CAP_INTSTS register

ADC_CTRL3			Page:1 / Address: 0x9D		ADC Control Register 3			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	DMA_INTE	A_WDG_INTE	REG_INTE
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2	DMA_INTE	R/W	DMA Finish interrupt enable 0: Disabled 1: Enabled	
1	A_WDG_INTE	R/W	Analog Watchdog interrupt enable on regular channel 0: Disabled 1: Enabled	
0	REG_INTE	R/W	Regular mode interrupt enable 0: Disabled 1: Enabled	

Table 5-53 ADC_CTRL3 register

ADC_CTRL4			Page:1 / Address: 0x9E		ADC Control Register 4			
Bit	7	6	5	4	3	2	1	0
Function	DMA_BUF_STATE	ADC_RDY	--	--	--	DMA_INTF	A_WDG_INTF	REG_INTF
Default	0	1	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7	DMA_BUF_STATE	R	DMA_BUFFER State 0: DMA write A buffer state or idle state 1: DMA write B buffer state	
6	ADC_RDY	R	ADC finish signal 0: ADC is idle or sample and hold or conversion 1: ADC data conversion done	
5:3	--	R/W	Reserved	
2	DMA_INTF	R/W	DMA finish interrupt flag Read : 0: DMA not finish or DMA no enable 1: DMA finish Write : 0: Clear this flag 1: No effect	
1	A_WDG_INTF	R/W	Analog Watchdog interrupt flag on regular channel Read : 0: No analog watch dog occurred 1: Analog watch dog occurred Write : 0: Clear this flag 1: No effect	
0	REG_INTF	R/W	Regular conversion interrupt flag Read : 0: No regular conversion was finished 1: Regular conversion has finished Write : 0: Clear this flag	

Bit	Function	Type	Description	Condition
			1: No effect	

Table 5-54 ADC_CTRL3 register

SYS_CTRL3			Page:0 / Address: 0xFC		System Control-3 Register			
Bit	7	6	5	4	3	2	1	0
Function	SW_RST_EN	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
Default	0	0	0	0	0	0	0	1
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7	SW_RST_EN	W	Software reset enable signal 0: Disables software reset 1: Enables software reset	
6	LVD_INT_EN	R/W	LVD interrupt enable 0: Disabled 1: Enabled	
5:4	LVD_SEL[1:0]	R/W	LVD voltage selection bits LVD_SEL[1:0] / Voltage: 00 → 2.6V 01 → 3.0V 10 → 3.4V 11 → 4.4V	
3	LVD_EN	R/W	LVD enable control 0: Disables LVD function 1: Enables LVD function	
1	LVR_SEL[1:0]	R/W	LVR voltage selection bits LVR_SEL[1:0] / Voltage: 00 → 2.4V 01 → 2.8V 10 → 3.2V 11 → 4.2V	
0	LVR_EN	R/W	LVR enable control 0: Disables LVR function 1: Enables LVR function It's recommended not to disable this bit.	

Table 5-55 SYS_CTRL3 register

SYS_CTRL4			Page:0 / Address: 0xFD		System Control-4 Register			
Bit	7	6	5	4	3	2	1	0
Function	POR_RST	WDOG_RST	--	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR
Default	1	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7	POR_RST	R/W	Power on reset indicated flag read: 0: Power on reset is inactive 1: Power on reset is active Write: 0: Clears this bit 1: No effect	
6	WDOG_RST	R/W	Watchdog reset indicated flag read: 0: Watchdog reset is inactive 1: Watchdog reset is active Write: 0: Clears this bit 1: No effect	
5	--	R/W	Reserved	
4	LVR_RST	R/W	LVR indicated flag read: 0: LVR is inactive 1: LVR is active Write: 0: Clears this bit 1: No effect	
3	LVD_INTF	R/W	LVD interrupt flag read: 0: LVD is inactive 1: LVD is active Write: 0: Clears this bit 1: No effect	
2	LVD_STS	R	LVD status flag. 0: LVD is inactive 1: LVD is active	
1	ADDR_ERR	R/W	FLASH access address over range flag. read: 0: FLASH access address is not over range 1: FLASH access address is over range Write: 0: Clears this bit 1: No effect	
0	ERR_WR	R/W	FLASH is illegal programming or erasing flag. This flag will be set to high when a programming or erasing is out of space or among lock_level range. read: 0: Legal programming or erasing 1: Illegal programming or erasing Write: 0: Clears this bit 1: No effect	

Table 5-56 SYS_CTRL4 register

EXT_INT_CTRL			Page: 0 / Address: 0xE5		External Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	DEBOUNCE_TIME[1:0]		--	--	--	--	EXT_INT1_EN	EXT_INT0_EN
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	DEBOUNCE_TIME	R/W	External interrupt de-bounce time select signal DEBOUNCE_TIME[1:0] / Clock Cycle: 00: 4 01: 37 10: 72 11: 142	
5:2	--	R/W	Reserved	
1	EXT_INT1_EN	R/W	External interrupt 1 enable signal that is mapped to P0_1. 0: Disabled 1: Enabled	
0	EXT_INT0_EN	R/W	External interrupt 0 enable signal that is mapped to P0_0. 0: Disabled 1: Enabled	

Table 5-57 EXT_INT_EN register

EXT_INT_EDGE			Page: 0 / Address: 0xE6		External Interrupt Edge Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	EXT_INT1_EDGE	EXT_INT0_EDGE
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	EXT_INT1_EDGE	R/W	External interrupt 1 trigger edge control signal 0: Falling edge 1: Rising edge	
0	EXT_INT0_EDGE	R/W	External interrupt 0 trigger edge control signal 0: Falling edge 1: Rising edge	

Table 5-58 EXT_INT_EDGE register

EXT_INT_FLAG			Common / Address: 0xE7		External Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	EXT_INT1_FLAG	EXT_INT0_FLAG
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	EXT_INT1_FLAG	R/W	External interrupt 1 flag Read: 0: External interrupt is not occurred 1: External interrupt is occurred Write: 0: Clears this bit 1: No effect	
0	EXT_INT0_FLAG	R/W	External interrupt 0 flag Read: 0: External interrupt is not occurred 1: External interrupt is occurred write: 0: Clears this bit 1: No effect	

Table 5-59 EXT_INT_FLAG register

5.7. Reset Sources

5.7.1. Introduction

There are six types of reset sources for the GPM8F3331B including Power-On Reset (POR), Low Voltage Reset (LVR), Pad Reset (RAD_RST), Watchdog Timer Reset (WDT_RST), Software Reset (S/W_RST) and FLASH Error Reset (ADDR_ERR_RST). **Figure 5-7** shows the block diagram of each reset source.

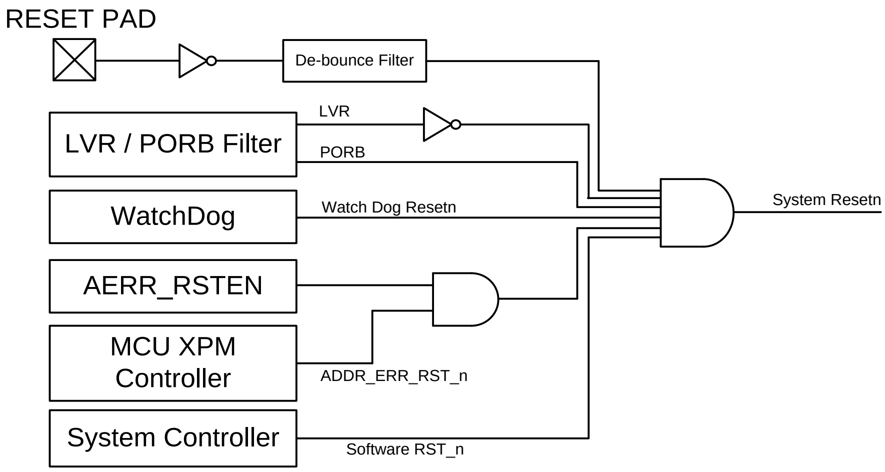


Figure 5-7 Reset sources

5.7.2. Power-On Reset (POR)

A POR is generated when VDD is rising from 0v. When VDD rises to an acceptable level (~1.2V), the power on reset circuit will start a power-on sequence. After that, the system starts to activate and will operate in target speed. The POR will reset the whole chip and registers.

5.7.3. Low Voltage Reset / Low Voltage Detect (LVR/LVD)

The on-chip Low Voltage Reset (LVR) circuitry forces the system entering reset state when power supplying voltage falls below the specific LVR trigger voltage. This function prevents MCU from working at an invalid operating voltage range.

To enable or disable this function, SYS_CTRL3[0] can be set. If this function is enabled, the LVR circuit will monitor power level while chip is operating. And the LVR voltage level can be 2.4V, 2.8V, 3.2V or 4.2V by setting SYS_CTRL3[2:1]. If the power is lower than the specific level for a specific period, the system reset will take place and go to initial state.

Allowing software to early notify that a power failure is about to occur, the LVD flag bit can be monitored. Built-in voltage detection circuit controls the LVD flag. The LVD flag is set while VDD supply is below LVD voltage and is cleared when VDD supply is over LVD voltage. The LVD voltage can be 2.6V, 3.0V 3.4V or 4.4V by setting SYS_CTRL3[5:4] bits.

5.7.4. Pad Reset (PAD_RST)

The GPM8F3331B provides an external pin to force the system returning to its initial status. The RESET pin is high active as shown in **Figure 5-8**. When the RESET pin equals to VDD over 300us, system will be forced to enter reset state, execute instruction from address 0x0000 and all registers go to default state.

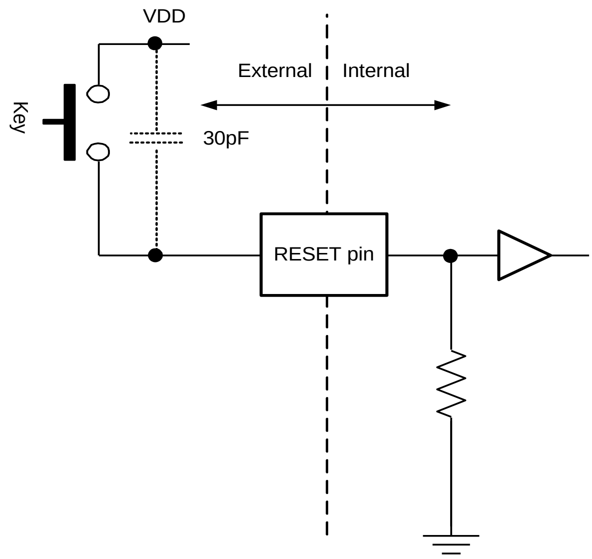


Figure 5-8 Pad reset circuit

5.7.5. Watchdog Timer Reset (WDT_RST)

On-chip watchdog circuitry makes the device entering reset state when MCU goes into unknown state and has no watchdog cleared information. This function prevents the MCU to be stuck in an abnormal condition. The WDT can be enabled or disabled through WDCON register bit 1. At any time prior to reaching its user selected terminal value, software can set the Reset Watchdog Timer (WDCON[0]) bit. If RWT is set before the timeout is reached, the timer will start over. If timeout is reached without RWT being set, the watchdog will reset the CPU. Hardware will automatically clear RWT after software sets it. When the reset occurs, the Watchdog Timer Reset Flag (SYSCON_CTRL4[6]) will automatically be set to indicate the cause of the reset, however software must clear this bit manually.

WDCON register is a timed access register that prevent it from accidental writes. KEYCODE is located at 0xEB. Correct sequence, 0xAA and 0x55, is required before writing to WDCON register. Reading from such register is not protected.

The Watchdog has four timeout selections based on the internal 32K clock frequency. The selections are a pre-selected number of clocks and can be set by CKCON[7:6]. In addition, CKCON[5] can be used to set these four timeout selections in fast mode or not. **Figure 5-9** shows the block diagram of Watchdog timer.

5.7.6. Other Reset Sources

Other reset sources includes Software Reset and FLASH Address Error Reset. Software Reset is occurred when writing KEY code to KEYCODE register (0xEB). The key codes are 0x8F, 0x32 and 0x50. The timing does not matter, but the key codes must be written in order before SW reset takes place. FLASH Address Error Reset is the reset when FLASH access addresses is out of FLASH space and AERR_RSTEN (SYS_CTRL6[2]) is set to 1. In GPM8F3331B, system supports five reset status flags that can be monitored by SYS_CTRL4 register, shown in **Table 5-64**

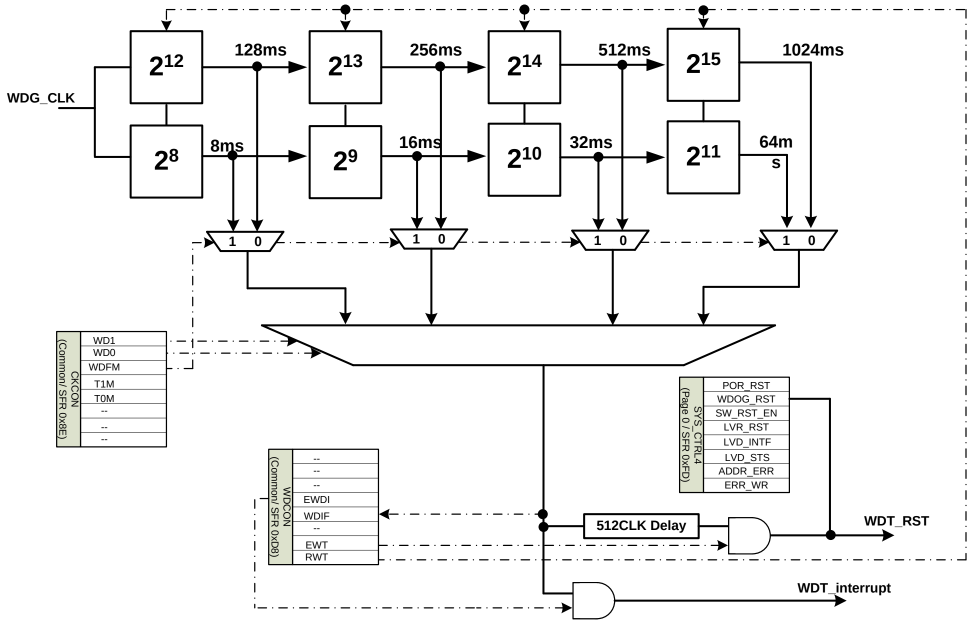


Figure 5-9 The block diagram of Watchdog timer

WDCON			**Common / Address: 0xD8**		**Watchdog Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	EWDI	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0
Keycode	AA /55							

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	EWDI	R/W	Enable Watchdog interrupt	
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disabled 1: Enabled	
0	RWT	R/W	Reset watchdog timer 0: NA 1: Reset	

Table 5-60 WDCON register

KEYCODE			**Common/Address: 0xEB**		**KEYCODE Register**			
Bit	7	6	5	4	3	2	1	0
Function	KC7	KC6	KC5	KC4	KC3	KC2	KC1	KC0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	KEYCODE[7:0]	W	KEYCODE register	

Table 5-61 KEYCODE register

Note 1: Some protected registers are needed to write correct key code to KEYCODE register before writing data to them.
Note 2: User must turn off global interrupt enable before using KEYCODE function.

CKCON			**Common/Address: 0x8E**		**Clock Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>WD[1:0]</td><td>R/W</td><td>Watchdog timeout selection bits
If WDFM=0:
<table>
<tr><td>WD[1:0]</td><td>Timeout</td></tr>
<tr><td>00</td><td>128ms</td></tr>
<tr><td>01</td><td>256ms</td></tr>
<tr><td>10</td><td>512ms</td></tr>
<tr><td>11</td><td>1024ms</td></tr>
</table>
If WDFM=1:
<table>
<tr><td>WD[1:0]</td><td>Timeout</td></tr>
<tr><td>00</td><td>8ms</td></tr>
<tr><td>01</td><td>16ms</td></tr>
<tr><td>10</td><td>32ms</td></tr>
<tr><td>11</td><td>64ms</td></tr>
</table></td><td></td></tr>
<tr><td>5</td><td>WDFM</td><td>R/W</td><td>Watchdog fast mode selection bit
0: watchdog fast mode disabled
1: watchdog fast mode enabled</td><td></td></tr>
<tr><td>4</td><td>T1M</td><td>R/W</td><td>Timer 1 clock source select signal. This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table>
<tr><td>T1M</td><td>T01_CK_SEL</td><td>Timer1 Clock</td></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>3</td><td>T0M</td><td>R/W</td><td>Timer 0 clock source select signal. This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table>
<tr><td>T0M</td><td>T01_CK_SEL</td><td>Timer0 Clock</td></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>2:0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-62 CKCON register

SYS_CTRL6			Common / Address: 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL[1:0]		UART0_IF_EN	T01_CK_SEL	--	ADDR_RSTEN	WDOG_CKEN	--
Default	0	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>UART_IF_SEL[1:0]</td><td>R/W</td><td>UART0 interface selection
00: TX is P14 , RX is P15 (default)
01: TX is P24 , RX is P25
10: TX is P30 , RX is P31
11: Reserved</td><td></td></tr>
<tr><td>5</td><td>UART0_IF_EN</td><td>R/W</td><td>UART0 interface enable signal
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>4</td><td>T01_CK_SEL</td><td>R/W</td><td>Timer0/1 clock source select signal. This bit is used combining with T0M/T1M of CKCON(0x8E).
<table>
<tr><td>TOM /T1M</td><td>T01_CK_SEL</td><td>Timer0/1 Clock</td></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>3</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>2</td><td>ADDR_RSTEN</td><td>R/W</td><td>FLASH address over range reset enable
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>1</td><td>WDOG_CKEN</td><td>R/W</td><td>Watchdog controller clock enable control bit
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-63 SYS_CTRL6 register

SYS_CTRL4			Page:0 / Address: 0xFD		System Control-4 Register			
Bit	7	6	5	4	3	2	1	0
Function	POR_RST	WDOG_RST	SW_RST_EN	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR
Default	1	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7	POR_RST	R/W	Power on reset indicated flag Read: 0: Power on reset is inactive 1: Power on reset is active Write: 0: Clears this bit 1: No effect	

Bit	Function	Type	Description	Condition
6	WDOG_RST	R/W	Watchdog reset indicated flag Read: 0: Watchdog reset is inactive 1: Watchdog reset is active Write: 0: Clears this bit 1: No effect	
5	SW_RST_EN	W	Software reset enable signal 0: Disables software reset 1: Enables software reset	
4	LVR_RST	R/W	LVR indicated flag Read: 0: LVR is inactive 1: LVR is active Write: 0: Clears this bit 1: No effect	
3	LVD_INTF	R/W	LVD interrupt flag Read: 0: LVD is inactive 1: LVD is active Write: 0: clears this bit 1: no effect	
2	LVD_STS	R	LVD status flag. 0: LVD is inactive 1: LVD is active	
1	ADDR_ERR	R/W	FLASH access address over range flag. Read: 0: FLASH access address is not over range 1: FLASH access address is over range Write: 0: Clears this bit 1: No effect	
0	ERR_WR	R/W	FLASH is illegal programming or erasing flag. This flag will be set to high when a programming or erasing is out of space or among lock_level range. read: 0: Legal programming or erasing 1: Illegal programming or erasing Write: 0: Clears this bit 1: No effect	

Table 5-64 SYS_CTRL4 register

5.8. I/O Ports

5.8.1. Introduction

GPM8F3331B supports up to 29 general propose I/O, including standard Port 0, Port 1, Port 2 and Port3. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input floating port. All the input ports can be programmable pull high/low by DIR, ATT and Px registers. The P0, P0_ID, P0_DIR and P0_ATT registers of Port 0 are controlled by 0x80, 0xA9 and SFRs 0xAA, 0xAB registers of page-0. The P1, P1_ID, P1_DIR and P1_ATT registers of Port 1 are controlled by 0x90, 0xB9 and SFRs 0xBA, 0xBB registers of page-0. The P2, P2_ID, P2_DIR and P2_ATT registers of Port 2 are controlled by 0xA0, 0xA1 and SFRs 0xA2, 0xA3 registers of page-0. The P3, P3_ID, P3_DIR and P3_ATT registers of Port 3 are controlled by 0xB0, 0xB1 and SFRs 0xB2, 0xB3 registers of page-0. The writing output data to the I/O port are performed via their corresponding SFRs P0(0x80), P1(0x90), P2(0xA0) and P3(0xB0). The reading data from the I/O port are performed via their corresponding SFRs P0_ID(0xA9), P1_ID(0xB9), P2_ID(0xA1) and P3_ID(0xB1). It is necessary that setting PX, PX_ATT, and PX_DIR register to ensure I/O State before using IO. Table 5-68 shows the truth table of analog pad and digital pad respectively. In GPM8F3331B, all the GPIO ports can be program to analog pad for special function. When GPIO port be program a analog pad, system will automatically switch to floating state. The detailed descriptions of analog function are in corresponding sections. The built-in pull high/low resistor is 50KΩ. In addition to, there is a register for slew rate control (Px_SR) of each port. The default state of Px_SR register is '0x00' without slew rate control function. **Figure 5-10** shows the block diagrams of the general purpose I/O.

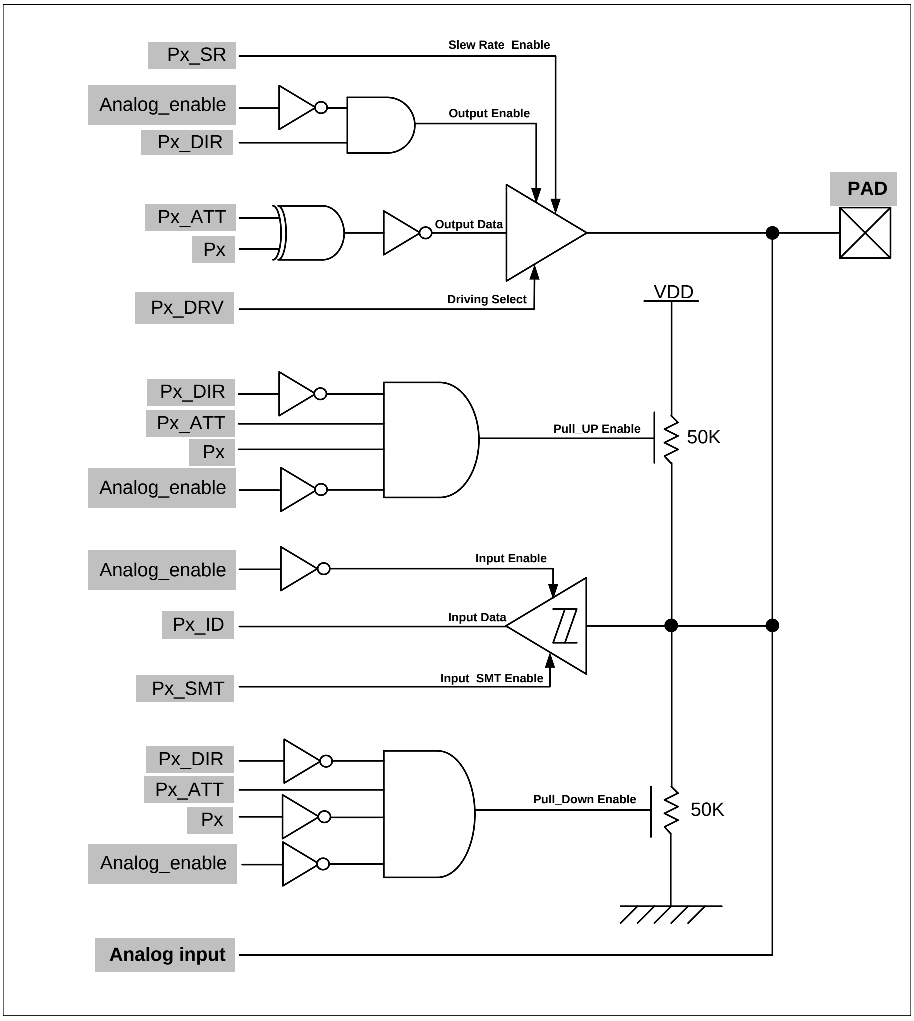


Figure 5-10 The block diagram of GPIO

Analog Enable	DIR	ATT	Px	Function	Description
0	0	0	0	Floating	Float (High Impendence)
0	0	0	1	Floating	Float (High Impendence)
0	0	1	0	Pull Low*	Input with pull low
0	0	1	1	Pull High	Input with pull high
0	1	0	0	Output High	Output with buffer (inverted -content of buffer register)
0	1	0	1	Output Low	Output with buffer (inverted -content of buffer register)
0	1	1	0	Output Low	Output with buffer
0	1	1	1	Output High	Output with buffer
1	X	X	X	Floating	Analog interface

Table 5-65 The truth table of GPIO

5.8.2. IO Special Function and GPIO Priority

The GPM8F3331B support special function and GPIO. The special function means ADC/ OP/ XTAL / I2C ….etc, when user use the special function, hardware will switch IO state automatic. When the user set more than two special functions simultaneously, hardware will select the high priority function as the GPIO function.

High Priority				->		Low Priority		
ADC / OP / CMP / XTAL / IO Charge	I2C	UART	TMA	TMB	TMC	SPI	ICE	GPIO
OP0_P	X	X	X	X	X	X	X	P00
OP0_N	X	X	X	X	X	X	X	P01
ADC_CH11 / CMP0_P	X	X	X	X	X	X	X	P02
ADC_CH10 / CMP0_N	X	X	X	X	X	X	X	P03
ADC_CH9 / CMP1_P	X	X	X	X	X	X	X	P04
ADC_CH8 / CMP1_N	X	X	X	X	X	X	X	P05
OP2_N	X	X	X	X	X	X	X	P06
OP1_O	X	X	X	X	X	X	X	P07
ADC_CH7 / OP1_CAP	X	X	X	X	X	X	X	P10
OP1_P	X	X	X	X	X	X	X	P11
ADC_CH5 / IO Charge	X	X	X	X	X	X	X	P12
ADC_CH4 / IO Charge	X	X	X	X	X	X	X	P13
ADC_CH3	O	O	X	X	O	X	X	P14
ADC_CH2	O	O	X	X	O	X	X	P15
ADC_CH1	X	X	X	X	X	X	X	P16
ADC_CH0	X	X	X	X	X	X	X	P17
X	X	X	O	O	X	X	X	P20
X	X	X	O	X	X	X	X	P21
X	X	X	O	X	X	X	X	P22
X	X	X	O	O	X	X	X	P23
X	X	O	X	O	X	X	X	P24
X	X	O	X	O	X	X	X	P25
X	X	X	X	X	X	X	X	P26
X	X	X	X	X	X	X	X	P27
XTAL	X	O	X	X	X	O	X	P30
XTAL	X	O	X	X	X	O	X	P31
X	X	X	X	X	X	O	X	P32
X	X	X	X	X	X	O	X	P33
X	X	X	X	X	X	X	O	P34

Table 5-66 IO priority table

5.8.3. GPIO Related Registers

P0			Common/Address: 0x80		Port0 Register			
Bit	7	6	5	4	3	2	1	0
Function	P0[7:0]							
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P0[7:0]	R/W	P0 is used to set IO output data only. Otherwise, it can also be used to configure the Port0 function.	

Table 5-67 P0 register

P1			Common/Address: 0x90		Port1 Register			
Bit	7	6	5	4	3	2	1	0
Function	P1[7:0]							
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P1[7:0]	R/W	P1 is used to set IO output data only. Otherwise, it can also be used to configure the Port1 function.	

Table 5-68 P1 register

P2			Common/Address: 0xA0		Port2 Register			
Bit	7	6	5	4	3	2	1	0
Function	P2[7:0]							
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P2[7:0]	R/W	P2 is used to set IO output data only. Otherwise, it can also be used to configure the Port2 function.	

Table 5-69 P2 register

P3			Common/Address: 0xB0		Port3 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3[4:0]				
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3[7:0]	R/W	P3 is used to set IO output data only. Otherwise, it can also be used to configure the Port3 function.	

Table 5-70 P3 register

P0_ID			Common/Address: 0xA9		Port0 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_ID[7:0]							
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7:0	P0_ID[7:0]	R/W	P0_ID is used to read-back I/O input state only.	

Table 5-71 P0_ID register

P1_ID			Common/Address: 0xB9		Port1 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_ID[7:0]							
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7:0	P1_ID[7:0]	R/W	P1_ID is used to read-back I/O input state only.	

Table 5-72 P1_ID register

P2_ID			Common/Address: 0xA1		Port2 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_ID[7:0]							
Default	X	X	X	X	X	X	X	X

Bit	Function	Type	Description	Condition
7:0	P2_ID[7:0]	R/W	P2_ID is used to read-back I/O input state only.	

Table 5-73 P2_ID register

P3_ID			Common/Address: 0xB1		Port3 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3_ID[4:0]				
Default	0	0	0	X	X	X	X	X

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_ID[4:0]	R/W	P3_ID is used to read-back I/O input state only.	

Table 5-74 P3_ID register

P0_DIR			Page: 0 / Address: 0xAA		Port0 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_DIR[7:0]	R/W	P0_DIR is use to configure the Port0 function. It indicates direction of corresponding I/O.	

Table 5-75 P0_DIR register

P1_DIR			Page: 0 / Address: 0xBA		Port1 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_DIR[7:0]	R/W	P1_DIR is use to configure the Port1 function. It indicates direction of corresponding I/O.	

Table 5-76 P1_DIR register

P2_DIR			Page: 0 / Address: 0xA2		Port2 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_DIR[7:0]	R/W	P2_DIR is use to configure the Port2 function. It indicates direction of corresponding I/O.	

Table 5-77 P2_DIR register

P3_DIR			Page: 0 / Address: 0xB2		Port3 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3_DIR[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_DIR[4:0]	R/W	P3_DIR is use to configure the Port3 function. That indicates direction of corresponding I/O.	

Table 5-78 P3_DIR register

P0_ATT			Page: 0 / Address: 0xAB		Port0 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_ATT[7:0]	R/W	P0_ATT can use to configure the Port0 function.	

Table 5-79 P0_ATT register

P1_ATT			Page: 0 / Address: 0xBB		Port1 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_ATT[7:0]	R/W	P1_ATT can use to configure the Port1 function.	

Table 5-80 P1_ATT register

P2_ATT			Page: 0 / Address: 0xA3		Port2 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_ATT[7:0]	R/W	P2_ATT can use to configure the Port2 function.	

Table 5-81 P2_ATT register

P3_ATT			Page: 0 / Address: 0xB3		Port3 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3_ATT[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_ATT[7:0]	R/W	P3_ATT can use to configure the Port3 function.	

Table 5-82 P3_ATT register

P0_DRV			Page: 0 / Address: 0xAC		Port0 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_DRV[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_DRV[7:0]	R/W	P0_DRV can use to configure the Port0 driving capability. 0: High driver 1: Normal Driver	

Table 5-83 P0_DRV register

P1_DRV			Page: 0 / Address: 0xBC		Port1 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DRV[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_DRV[7:0]	R/W	P1_DRV can use to configure the Port1 driving capability. 0: High driver 1: Normal Driver	

Table 5-84 P1_DRV register

P2_DRV			Page: 0 / Address: 0xA4		Port2 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_DRV[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_DRV[7:0]	R/W	P2_DRV can use to configure the Port2 driving capability. 0: High driver 1: Normal Driver	

Table 5-85 P2_DRV register

P3_DRV			Page: 0 / Address: 0xB4		Port3 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3_DRV[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_DRV[4:0]	R/W	P3_DRV can configure the Port3 driving capability. 0: High driver 1: Normal Driver	

Table 5-86 P3_DRV register

P0_SR			Page: 0 / Address: 0xAD		Port0 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_SR[7:0]	R/W	P0_SR can use to configure the Port0 output slew rate,	

Table 5-87 P0_SR register

P1_SR			Page: 0 / Address: 0xBD		Port1 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_SR[7:0]	R/W	P1_SR can configure the Port1 output slew rate,	

Table 5-88 P1_SR register

P2_SR			Page: 0 / Address: 0xA5		Port2 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_SR[7:0]	R/W	P2_SR can configure the Port2 output slew rate,	

Table 5-89 P2_SR register

P3_SR			**Page: 0 / Address: 0xB5**		**Port3 Slew Rate Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3_SR[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_SR[4:0]	R/W	P3_SR can configure the Port3 output slew rate,	

Table 5-90 P3_SR register

P0_SMT			**Page: 0 / Address: 0xAE**		**Port0 Schmitt Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	P0_SMT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_SMT[7:0]	R/W	P0 input Schmitt trigger control	

Table 5-91 P0_SMT register

P1_SMT			**Page: 0 / Address: 0xBE**		**Port1 Schmitt Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	P1_SMT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_SMT[7:0]	R/W	P1 input Schmitt trigger control	

Table 5-92 P1_SMT register

P2_SMT			**Page: 0 / Address: 0xA6**		**Port2 Schmitt Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	P2_SMT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_SMT[7:0]	R/W	P2 input Schmitt trigger control	

Table 5-93 P2_SMT register

P3_SMT			**Page: 0 / Address: 0xB6**		**Port3 Schmitt Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3_SMT[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_SMT[4:0]	R/W	P3 input Schmitt trigger control	

Table 5-94 P3_SMT register

5.9. Timer Module

5.9.1. Introduction

GPM8F3331B is equipped with five timers. They are Timer 0, Timer 1, Timer A, Timer B and Timer C respectively. In addition, Timer A, Timer B also features Compare/Capture/PWM function. Timer C features Capture function. The Timer 0 and Timer 1 are up-count timers with 16-bit resolution. The Timer A, Timer B, Timer C are down-count timers and with 16-bit resolution. Each timer's function is described in the following sections.

5.9.2. Timer 0/1

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0(0x8C), TL0(0x8A), TH1(0x8D), TL1(0x8B). Timer 0 and Timer 1 work in the same three modes except for mode 3 and the related control registers are TMOD(0x89), TCON(0x88) and CKCON(0x8E) registers. In the timer mode, timer registers are incremented every 1/2/4/8 SYSCLK periods depends on CKCON(0x8E) and SYS_CTRL6(0xFF) setting, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

5.9.2.1. Timer 0: Mode 0 (13-Bit Timer/Counter)

In this mode, Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TR0(TCON[4]) = 1. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Figure 5-11 shows the block diagram of Timer 0 for Mode 0.

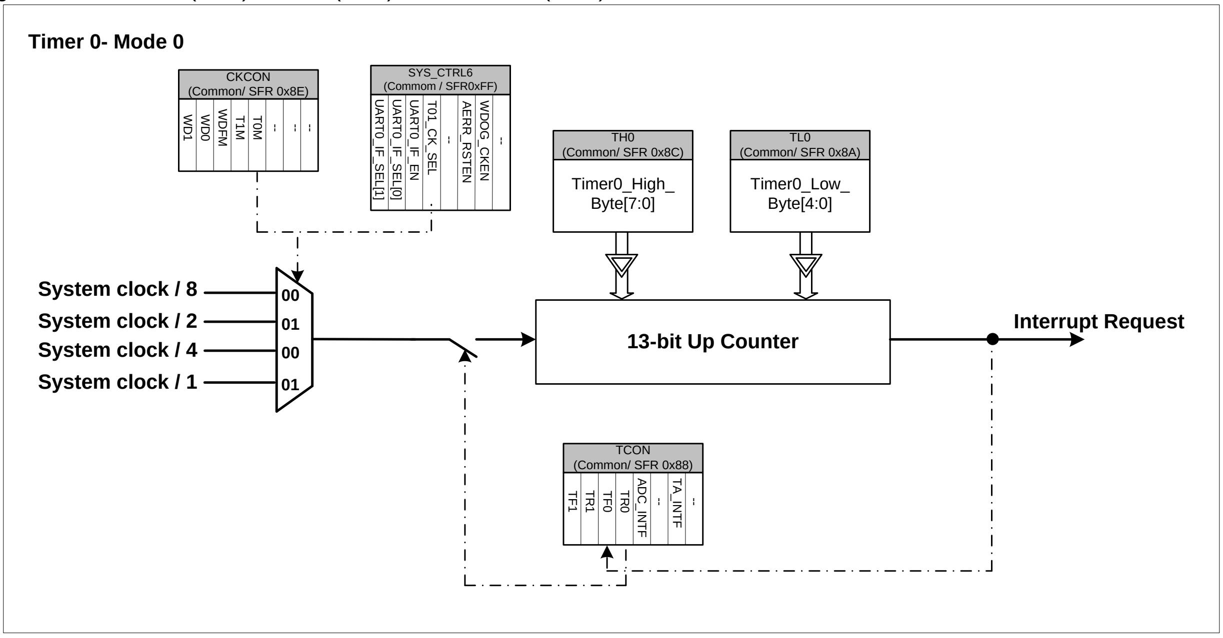


Figure 5-11 The block diagram of Timer 0 for Mode 0

5.9.2.2. Timer 0: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-12.

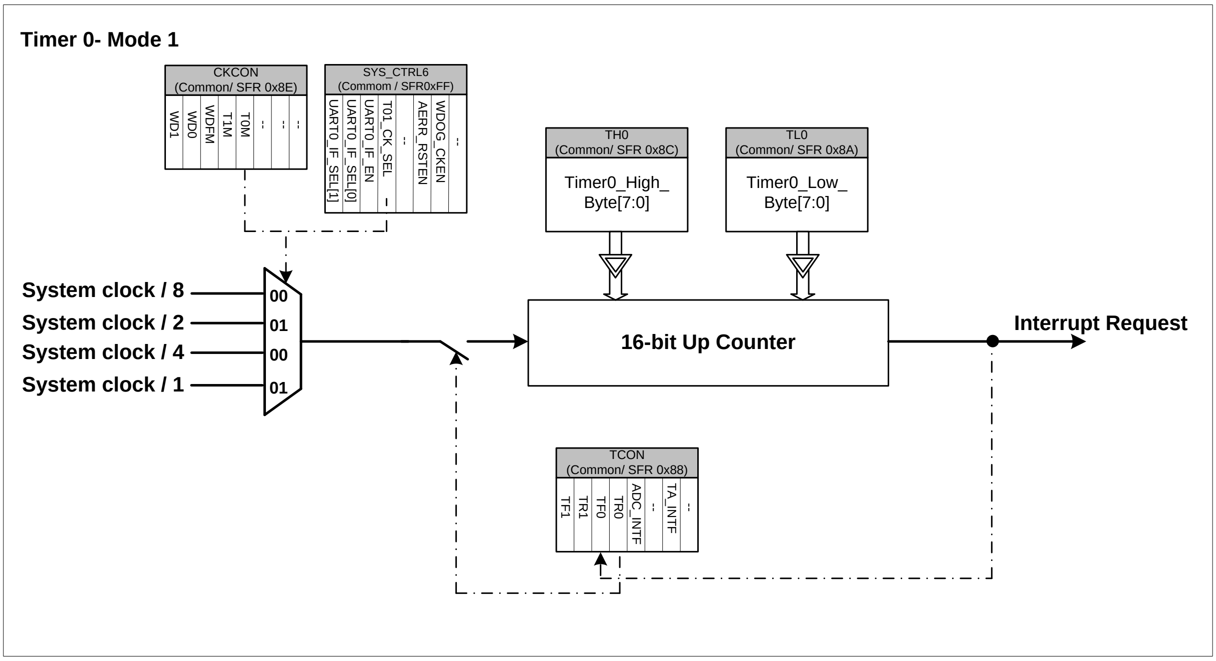


Figure 5-12 The block diagram of Timer 0 for Mode 1

5.9.2.3. Timer 0: Mode 2 (8-bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

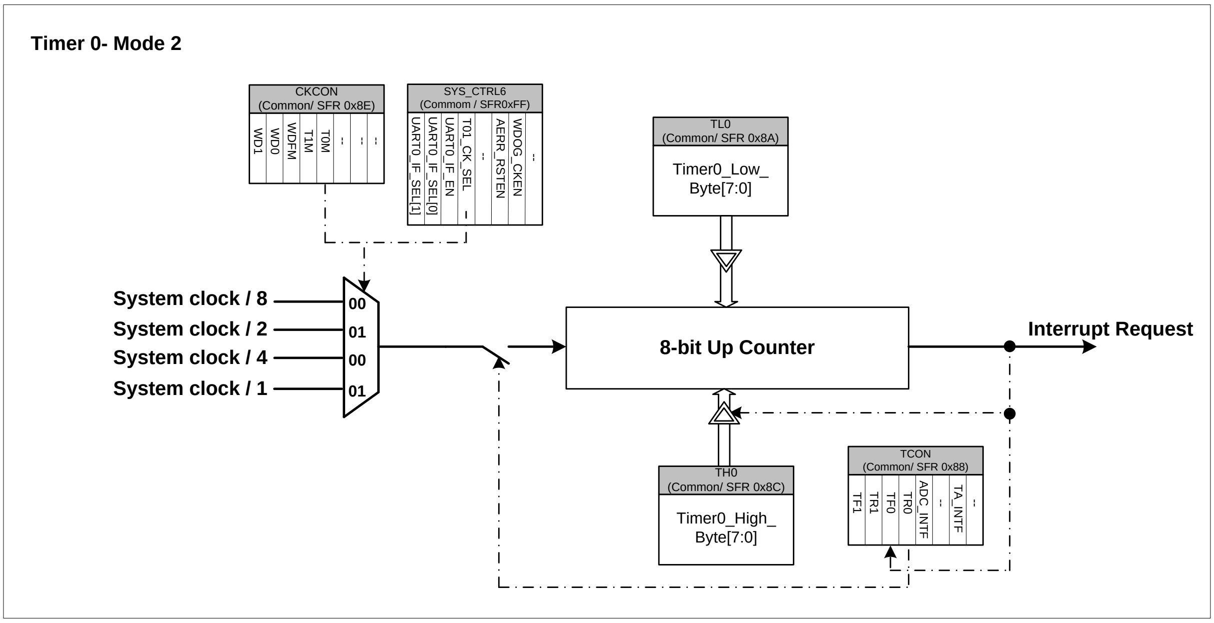


Figure 5-13 The block diagram of Timer 0 for Mode 2

5.9.2.4. Timer 0: Mode 3 (Two 8-Bit Timers/Counters)

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The block diagram for Mode 3 on Timer 0 is shown in Figure 5-14. TL0 uses the Timer 0 control bits: CT0, GATE0, TR0, and TF0. TH0 is locked into a timer function and uses the TR1 and TF1 flags from Timer 1 and controls Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

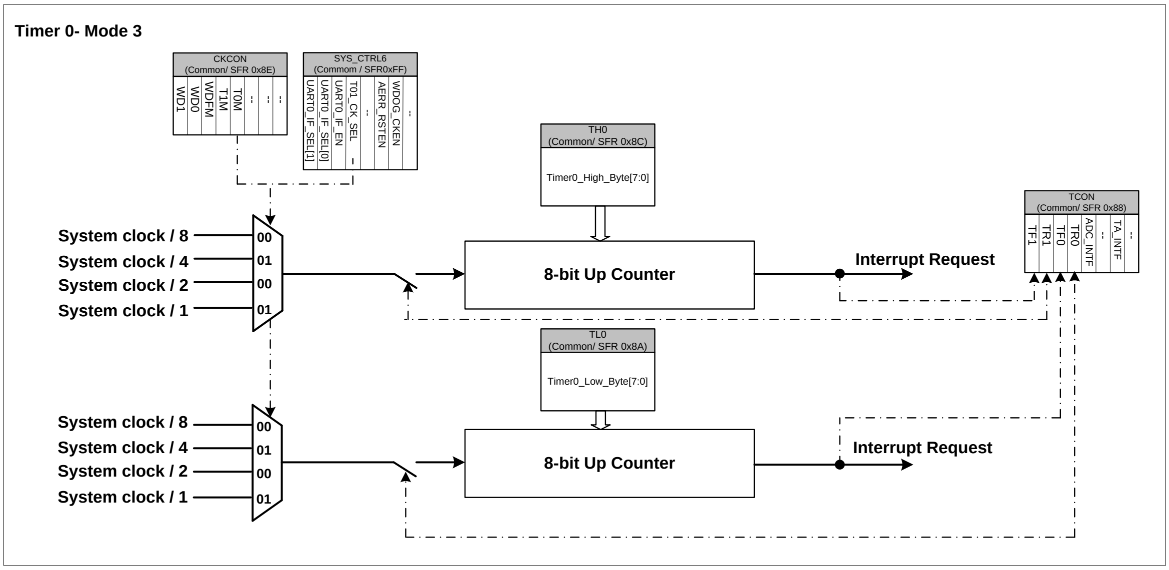


Figure 5-14 The block diagram of Timer 0 for Mode 3

5.9.2.5. Timer 1: Mode 0 (13-Bit Timer/Counter)

In this mode, the Timer 1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TR1(TCON[6]) = 1 and the input source is 32KHz clock. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Figure 5-15 shows the block diagram of Timer1 for Mode 0.

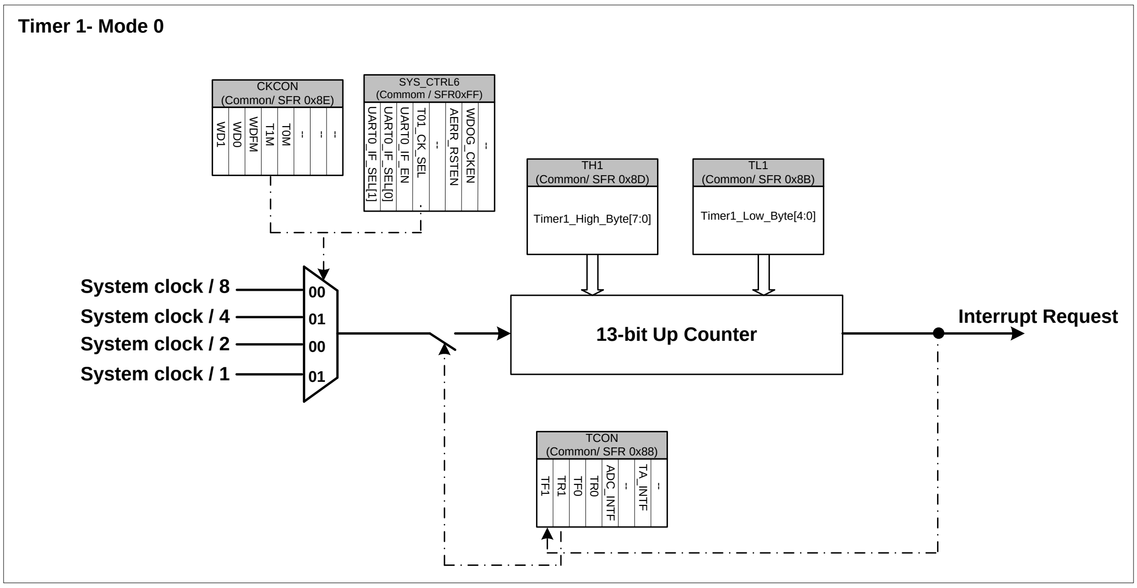


Figure 5-15 The block diagram of Timer 1 for Mode 0

5.9.2.6. Timer 1: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-16.

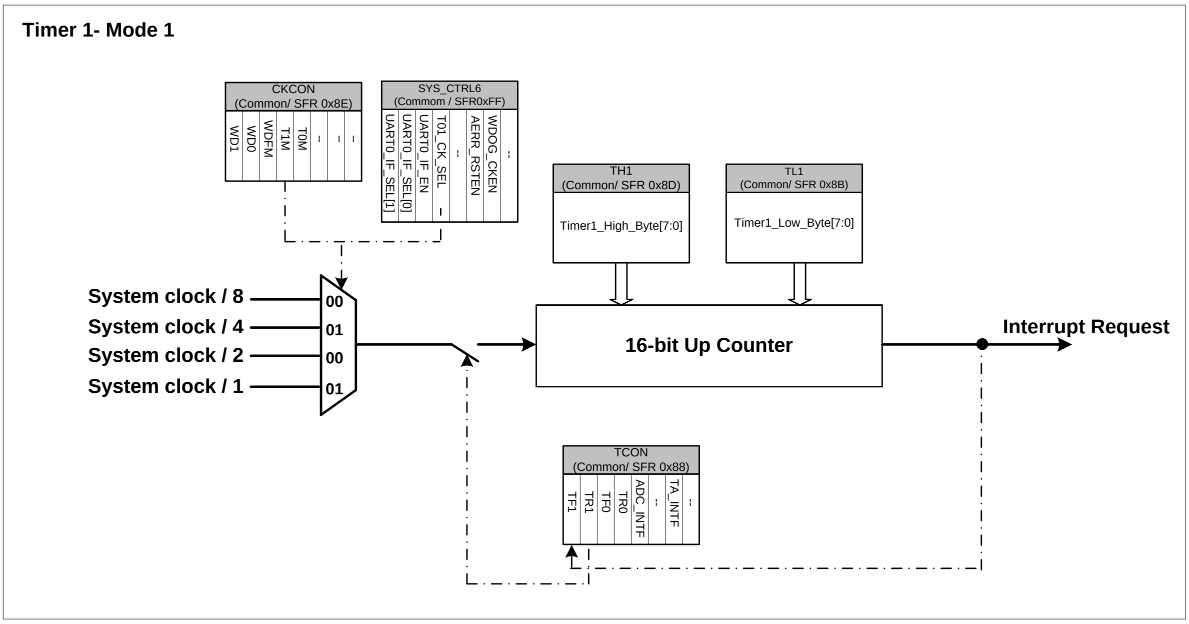


Figure 5-16 The block diagram of Timer 1 for Mode 1

5.9.2.7. Timer 1: Mode 2 (8-Bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in Figure 5-17. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

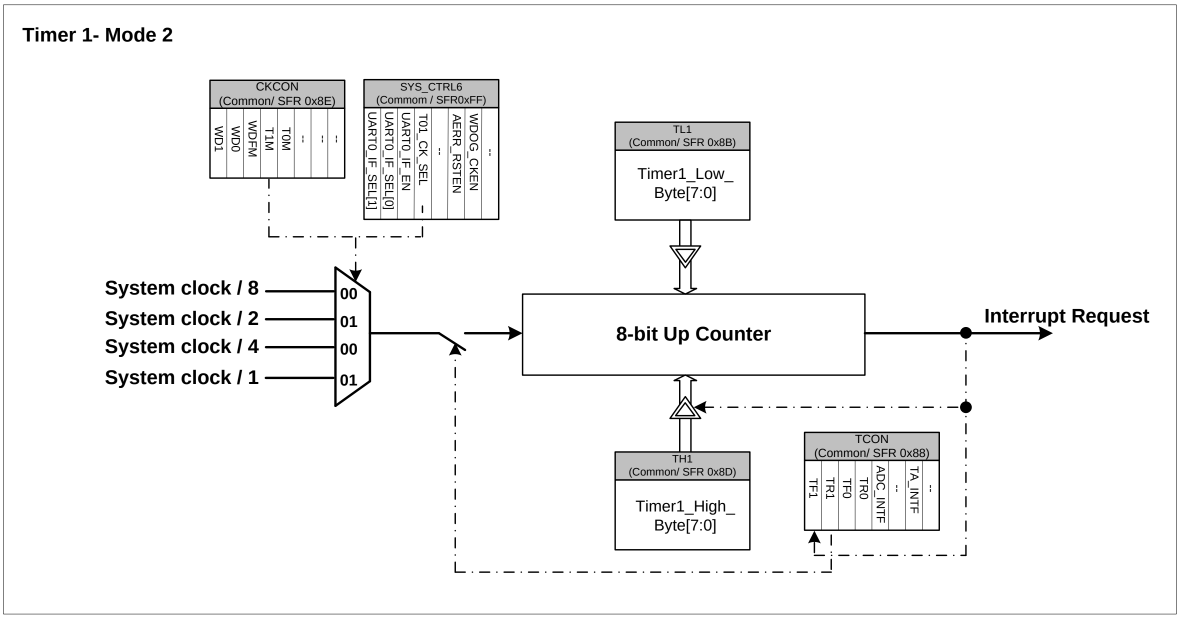


Figure 5-17 The block diagram of Timer 1 for Mode 2

5.9.2.8. Timer 1: Mode 3

Timer 1 in Mode 3 is has no timer function. The effect is the same as setting TR1=0.

5.9.2.9. Timer 0 / 1 Related Register

TH0			**Common /Address: 0x8C**		**Timer0 High Byte Register**			
Bit	7	6	5	4	3	2	1	0
Function	TH0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH0[7:0]	R/W	Timer 0 Load value – high byte	

Table 5-95 TH0 register

TL0			**Common /Address: 0x8A**		**Timer0 Low Byte Register**			
Bit	7	6	5	4	3	2	1	0
Function	TL0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL0[7:0]	R/W	Timer 0 Load value – low byte	

Table 5-96 TL0 register

TH1			**Common /Address: 0x8D**		**Timer1 High Byte Register**			
Bit	7	6	5	4	3	2	1	0
Function	TH1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH1[7:0]	R/W	Timer 1 Load value – high byte	

Table 5-97 TH1 register

TL1			**Common /Address: 0x8B**		**Timer1 Low Byte Register**			
Bit	7	6	5	4	3	2	1	0
Function	TL1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL1[7:0]	R/W	Timer 1 Load value – low byte	

Table 5-98 TL1 register

TMOD			**Common /Address: 0x89**		**Timer0/1 Control Mode Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	M11	M10	--	--	M01	M00
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:4	M1[1:0]	R/W	Mode select bits of timer 1, which is tabled as Table 5-100	
3:2	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
1:0	M0[1:0]	R/W	Mode select bits of timer 0, which is tabled as Table 5-100	

Table 5-99 TMOD register

M1	M0	Mode	Function description
0	0	0	TH0/1 operates as 8-bit timer/counter with a divide by 32 pre-scaling served by lower 5-bit of TL0/1.
0	1	1	16-bit timer/counter. TH0/1 and TL0/1 are cascaded
1	0	2	TL0/1 operates as 8-bit timer/counter with 8-bit auto-reload by TH0/1
1	1	3	TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table 5-100 Four modes of Timer 0 and Timer 1

TCON			Common /Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	ADC_INTF	--	TA_INTF	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: Disabled 1: Enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: Disabled 1: Enabled	
3	ADC_INTF	R/W	ADC interrupt flag	
2	--	R/W	Reserved	
1	TA_INTF	R/W	Timer A interrupt flag	
0	--	R/W	Reserved	

Table 5-101 TCON register

CKCON			Common /Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0: WD[1:0] / Timeout: 00 = 128ms 01 = 256ms 10 = 512ms 11 = 1024ms If WDFM=1:	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td></td><td></td><td></td><td><table><tr><td>WD[1:0]</td><td>Timeout</td></tr><tr><td>00</td><td>8ms</td></tr><tr><td>01</td><td>16ms</td></tr><tr><td>10</td><td>32ms</td></tr><tr><td>11</td><td>64ms</td></tr></table></td><td></td></tr>
<tr><td>5</td><td>WDFM</td><td>R/W</td><td>Watchdog fast mode selection bit
0: Watchdog fast mode disabled
1: Watchdog fast mode enabled</td><td></td></tr>
<tr><td>4</td><td>T1M</td><td>R/W</td><td>Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).<table><tr><td>T1M</td><td>T01_CK_SEL</td><td>Timer1 Clock</td></tr><tr><td>0</td><td>0</td><td>System Clock / 8</td></tr><tr><td>0</td><td>1</td><td>System Clock / 2</td></tr><tr><td>1</td><td>0</td><td>System Clock / 4</td></tr><tr><td>1</td><td>1</td><td>System Clock / 1</td></tr></table></td><td></td></tr>
<tr><td>3</td><td>T0M</td><td>R/W</td><td>Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).<table><tr><td>T0M</td><td>T01_CK_SEL</td><td>Timer0 Clock</td></tr><tr><td>0</td><td>0</td><td>System Clock / 8</td></tr><tr><td>0</td><td>1</td><td>System Clock / 2</td></tr><tr><td>1</td><td>0</td><td>System Clock / 4</td></tr><tr><td>1</td><td>1</td><td>System Clock / 1</td></tr></table></td><td></td></tr>
<tr><td>2:0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-102 CKCON register

<table>
<tr><th colspan="3">SYS_CTRL6</th><th colspan="2">Common / Address: 0xFF</th><th colspan="4">System Control-6 Register</th></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Function</td><td colspan="2">UART0_IF_SEL</td><td>UART0_IF_EN</td><td>T01_CK_SEL</td><td>--</td><td>ADDR_RSTEN</td><td>WDOG_CKEN</td><td>--</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Key Code</td><td colspan="8">0x8F / 0x32 / 0x50</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>UART_IF_SEL[1:0]</td><td>R/W</td><td>UART0 interface select
00: TX is P14 , RX is P15 (default)
01: TX is P24 , RX is P25
10: TX is P30 , RX is P31
11: Reserved</td><td></td></tr>
<tr><td>5</td><td>UART0_IF_EN</td><td>R/W</td><td>UART0 interface enable signal.
0: Disabled
1: Enabled</td><td></td></tr>
<tr><td>4</td><td>T01_CK_SEL</td><td>R/W</td><td>Timer0/1 clock source select signal. This bit is used combining with T0M/T1M of CKCON(0x8E).<table><tr><td>T0M /T1M</td><td>T01_CK_SEL</td><td>Timer0/1 Clock</td></tr><tr><td>0</td><td>0</td><td>System Clock / 8</td></tr><tr><td>0</td><td>1</td><td>System Clock / 2</td></tr><tr><td>1</td><td>0</td><td>System Clock / 4</td></tr></table></td><td></td></tr>
</table>

Bit	Function	Type	Description	Condition
			1 | 1 | System Clock / 1	
3	--	R/W	Reserved	
2	ADDR_RSTEN	R/W	FLASH address over range reset enable 0: Disabled 1: Enabled	
1	WDOG_CKEN	R/W	Watchdog controller clock enable control bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-103 The SYS_CTRL6 register

5.9.3. Timer A

The Timer A, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture/PWM feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

5.9.3.1. Timer / Counter mode

In timer / counter function, that have up to 8 clock source can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The Figure 5-18 shows the block diagram of counter / timer function for Timer A. When Timer A rolls over from pre-load data (TMA_PLOAD_H/L) to 0, not only TMA_INTF is set but also Timer A registers is loaded with the 16-bit value from TMA_PLOAD_H/L register. Required TMA_PLOAD_H/L value can be preset by software.

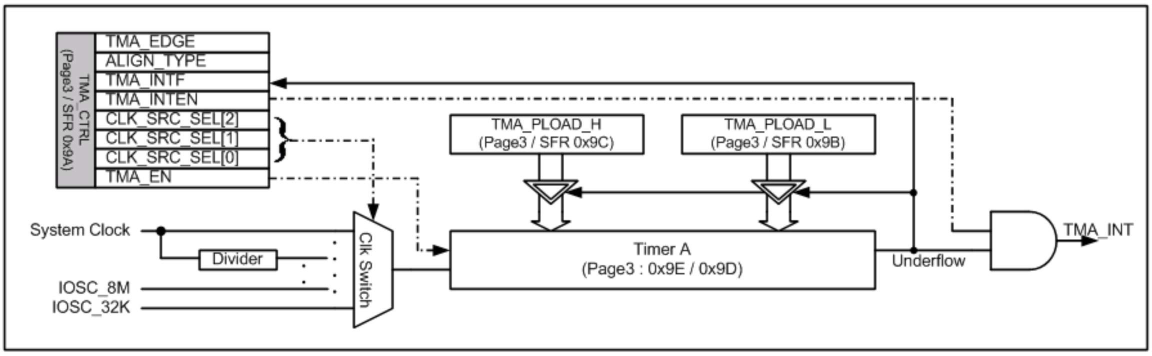


Figure 5-18 The block diagram of counter / timer function for Timer

5.9.3.2. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer A registers (TMA_H and TMA_L) when an external event is triggered. Figure 5-19 shows functional diagrams of the Timer A capture function.

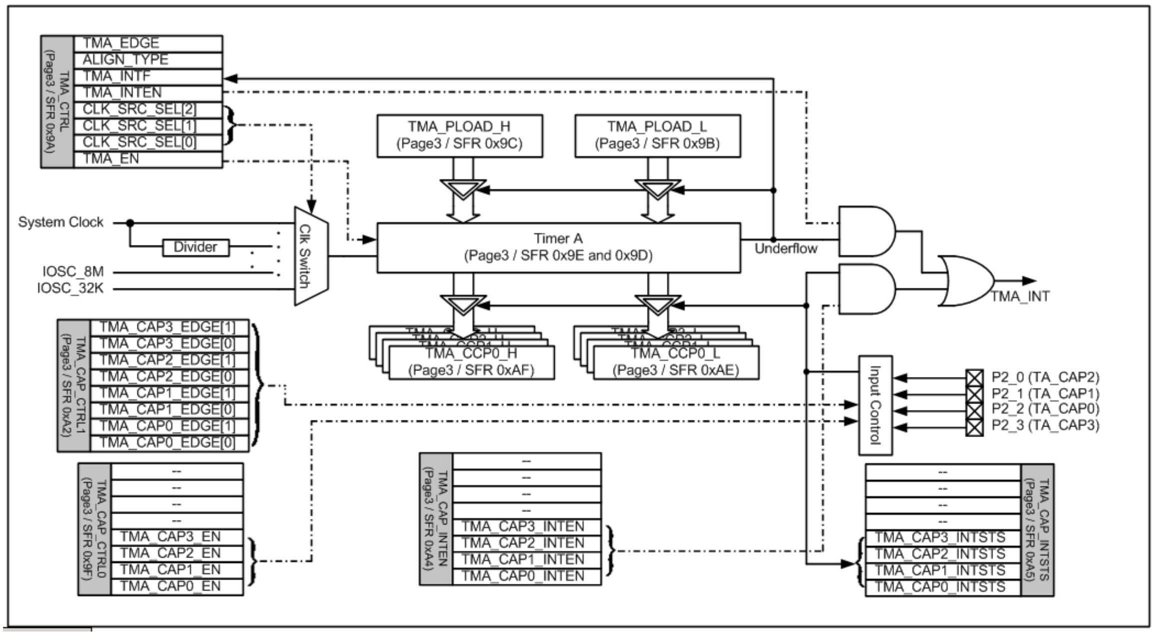


Figure 5-19 The block diagram of Timer A capture mode

5.9.3.3. PWM functions

The Timer A consists of four sets PWM function. When the TMA_PWMx_EN is enabled, the PWM output will toggle at the TMA_H/L are lesser or greater than TMA_CCPx_H/L (TMA_END_HL) value. About Timer count policy, there are two options can be choice between edge and center alignment. In edge alignment, the counter decrease counter value per clock cycle. Hardware will auto re-load TMA_PLOAD_H/L value to counter when counter is underflow. In center alignment, the counter is executing down count first and executing up-count next. There are two output mode of PWM output pin: independent and complement mode. In each mode, user can change output polarity with TMA_PWM_CTRL2 randomly. Figure 5-20 shows functional diagrams of the Timer A PWM function, and Figure 5-21 to Figure 5-27 are PWM operating waveform.

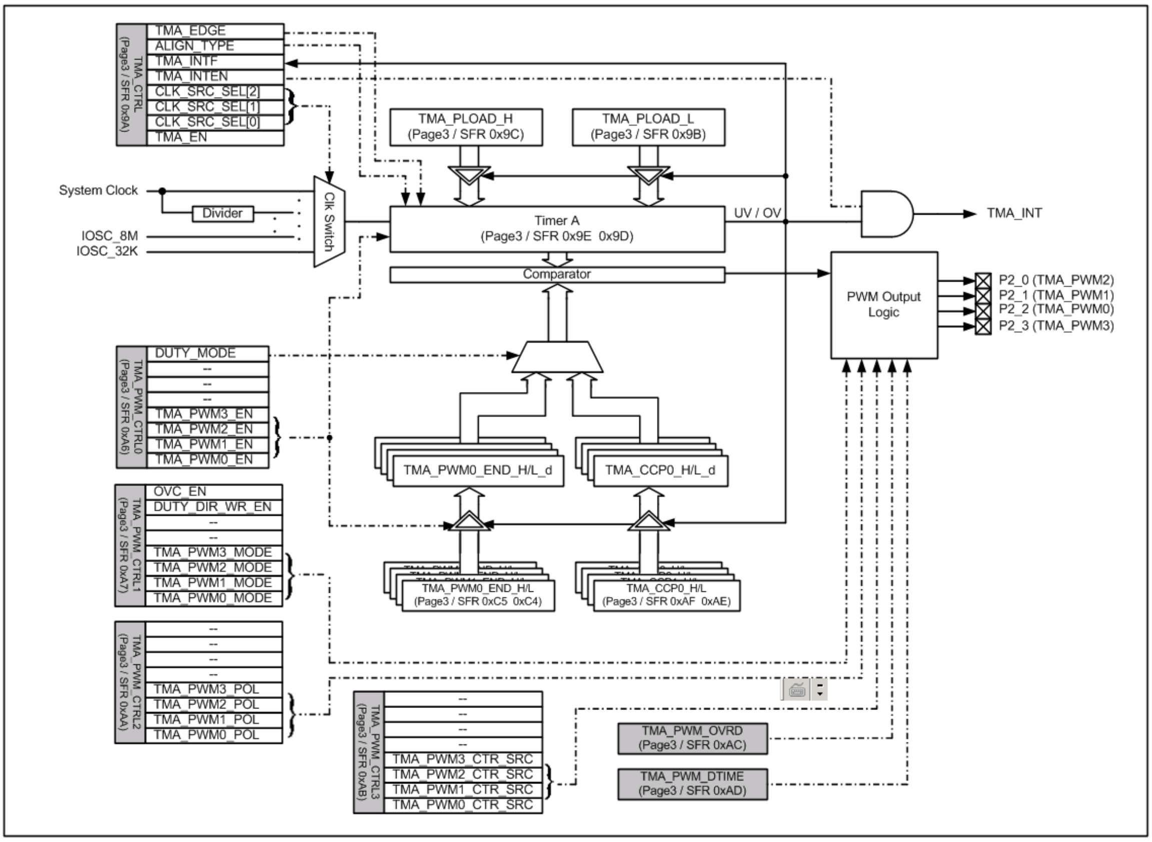


Figure 5-20 The block diagram of Timer A PWM mode

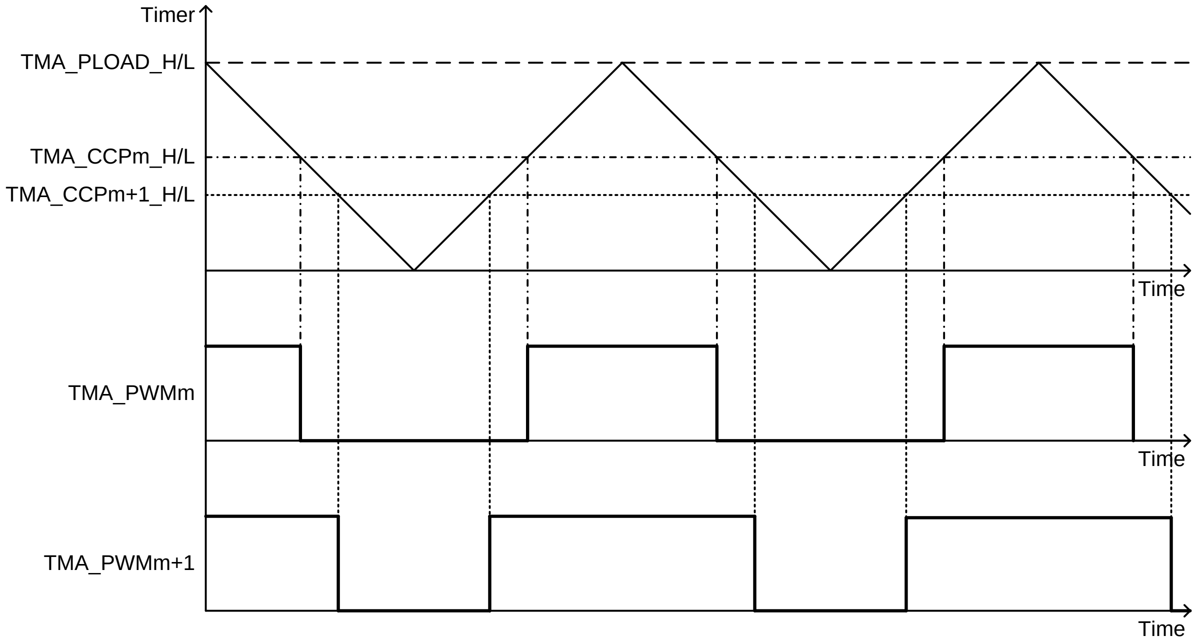


Figure 5-21 The waveform of Timer A PWM without dead time (ALIGN_TYPE: 1 / DUTY_MODE: 0 / TMA_PWMx_MODE: 0 ; m=0/2)

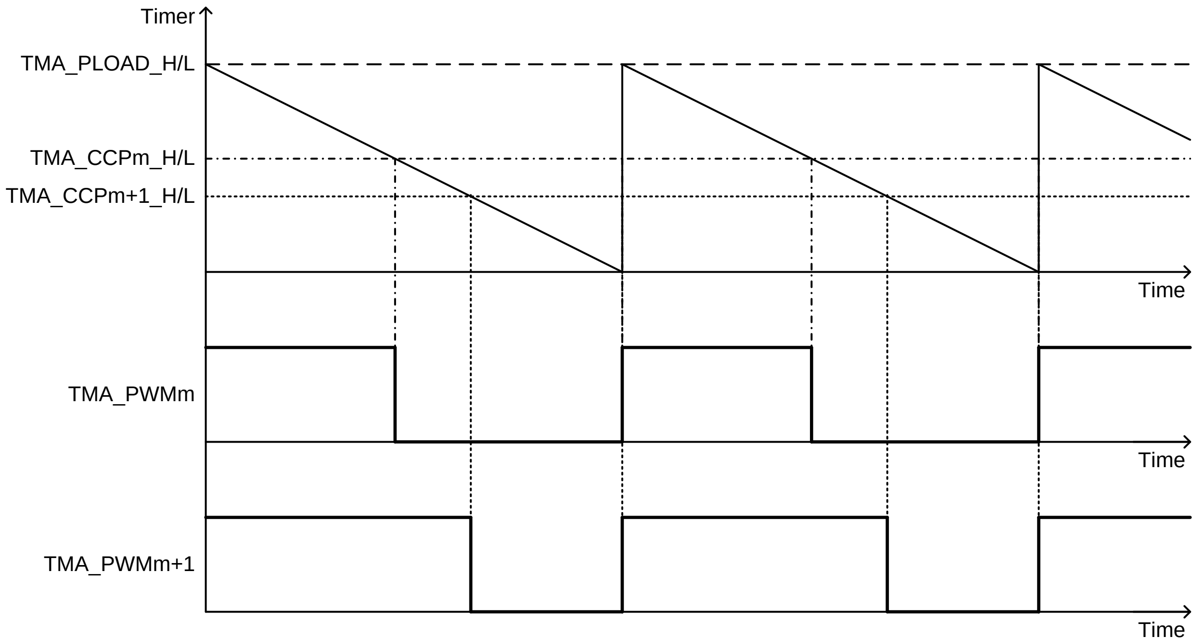


Figure 5-22 The waveform of Timer A PWM without dead time (ALIGN_TYPE: 0 / DUTY_MODE: 0 / TMA_PWMx_MODE: 0 ; m=0/2)

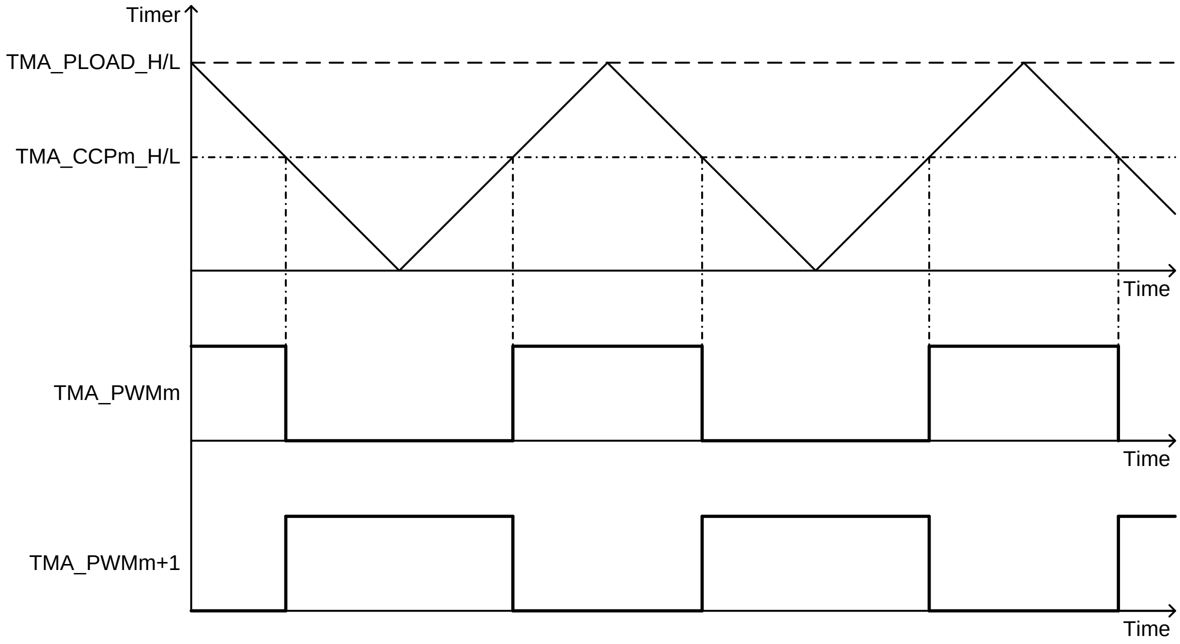


Figure 5-23 The waveform of Timer A PWM without dead time (ALIGN_TYPE: 1 / DUTY_MODE: 0 / TMA_PWMx_MODE: 1 ; m=0/2)

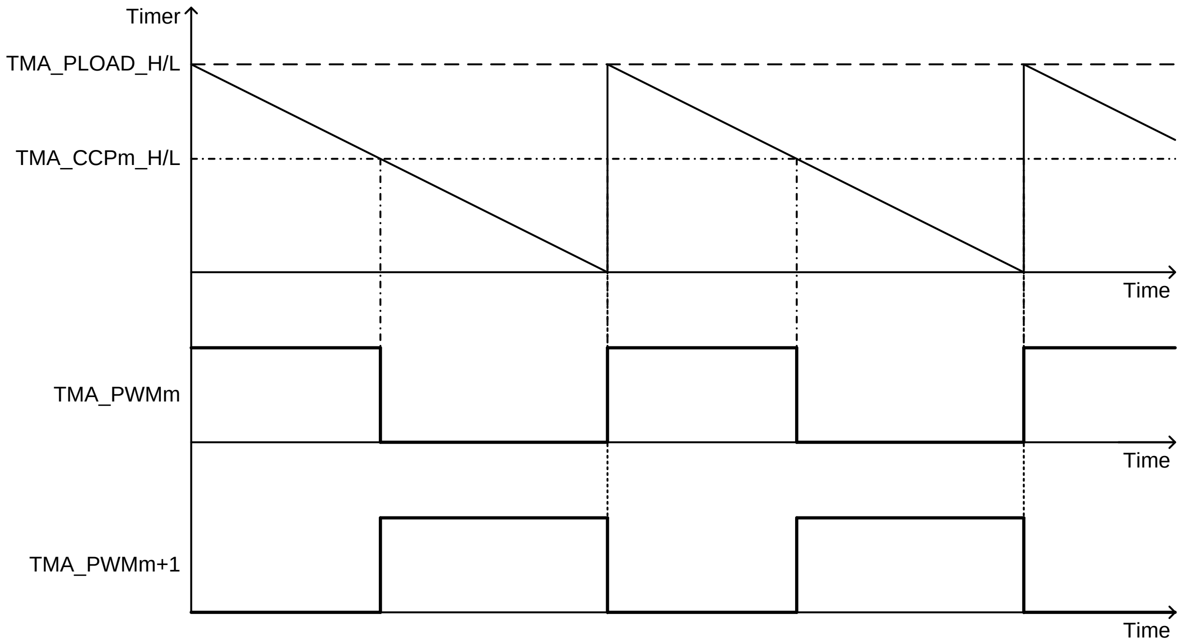


Figure 5-24 The waveform of Timer A PWM without dead time (ALIGN_TYPE: 0 / DUTY_MODE: 0 / TMA_PWMx_MODE: 1 ; m=0/2)

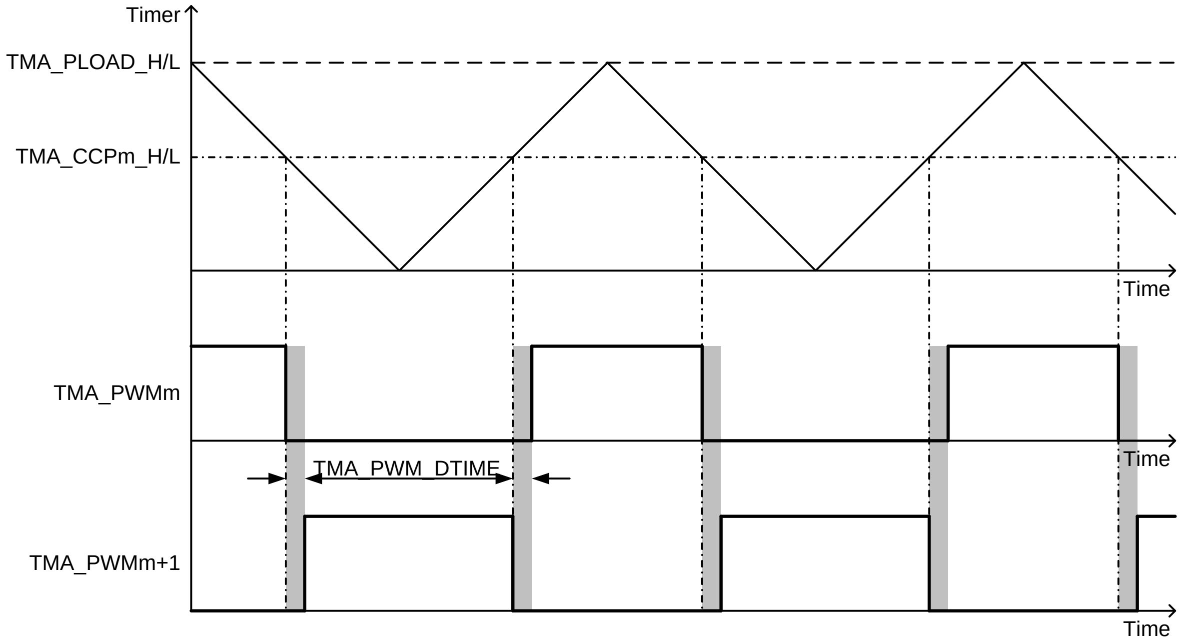


Figure 5-25 The waveform of Timer A PWM with dead time (ALIGN_TYPE: 1 / DUTY_MODE: 0 / TMA_PWMx_MODE: 1 ; m=0/2)

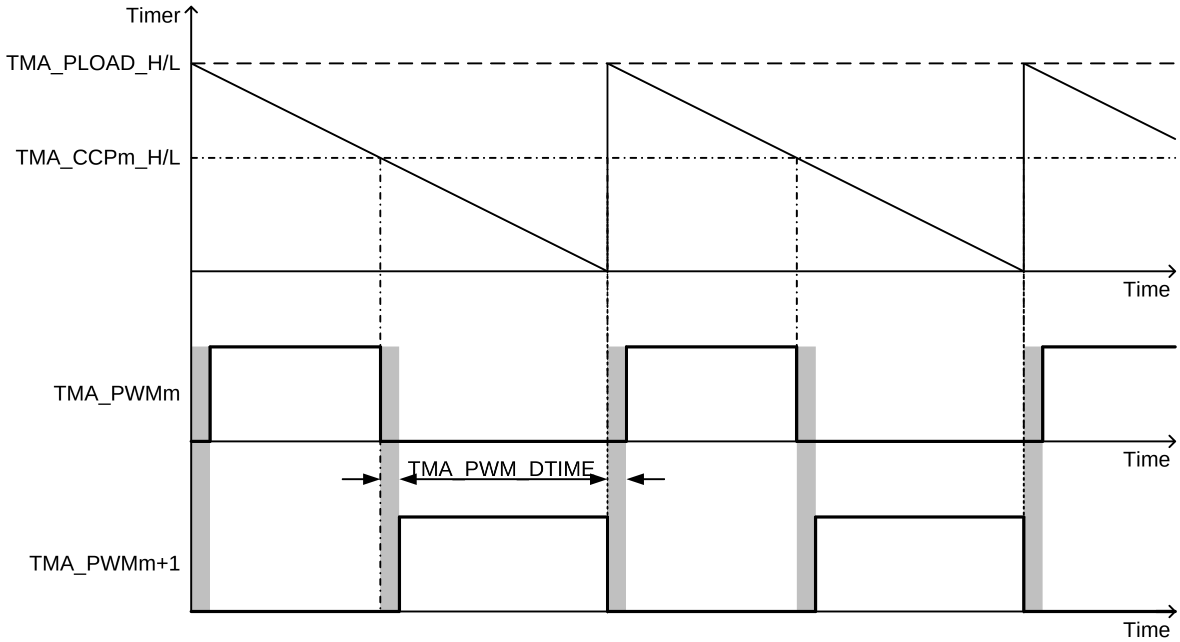


Figure 5-26 The waveform of Timer A PWM with dead time (ALIGN_TYPE: 0 / DUTY_MODE: 0 / TMA_PWMx_MODE: 1 ; m=0/2)

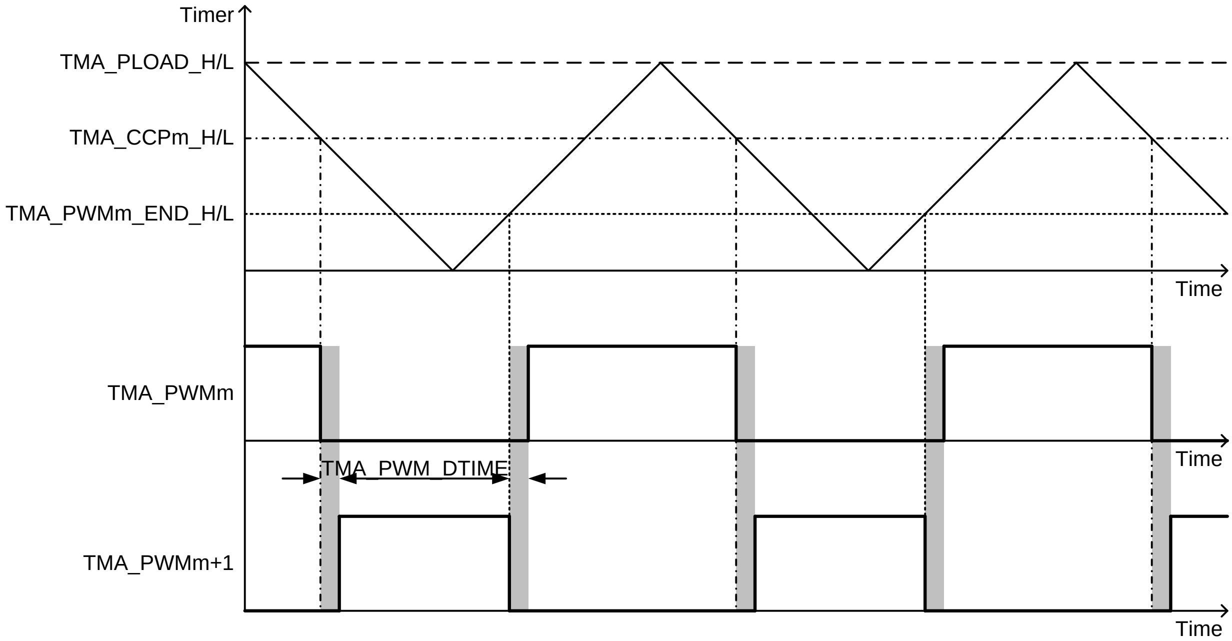


Figure 5-27 The waveform of Timer A PWM with dead time (ALIGN_TYPE: 1 / DUTY_MODE: 1 / TMA_PWMx_MODE: 1 ; m=0/2)

5.9.3.4. Timer A Related Registers

TMA_CTRL			Page: 3 / Address: 0x9A		Timer A Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_EDGE	ALIGN_TYPE	TMA_INTF	TMA_INTEN	CLK_SRC_SEL[2:0]			TMA_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMA_EDGE	R	Timer A up/down count edge indication. 0: Falling edge 1: Rising edge	
6	ALIGN_TYPE	R/W	0: Edge align 1: Center align	
5	TMA_INTF	R/W	Timer A interrupt flag. Read: 0: Idle / busy 1: Timer A interrupt trigger Write : 0: Clears this bit 1: No effect	
4	TMA_INTEN	R/W	Timer A interrupt enable control bit 0: Disabled 1: Enabled	
3:1	CLK_SRC_SEL	R/W	Timer A input clock source selection control bit CLK_SRC_SEL[2:0] — Clock Source 000 — System clock 001 — System clock / 2 010 — System clock / 4 011 — System clock / 8	

Bit	Function	Type	Description	Condition
			100 System clock / 16 101 System clock / 32 110 IOSC_8M 111 IOSC_32K Note: when CLK_SRC_SEL select IOSC8M , the system clock must faster more 2 times than IOSC8M.	
0	TMA_EN	R/W	Timer A enable control bit. 0: Disabled 1: Enabled	

Table 5-104 TMA_CTRL register

TMA_PLOAD_L			**Page: 3 / Address: 0x9B**		**Timer A Pre-Load Register - Low Byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PLOAD_L[7:0]	R/W	Timer A pre-load data or PWM period data register – low byte	

Table 5-105 TMA_PLOAD_L register

TMA_PLOAD_H			**Page: 3 / Address: 0x9C**		**Timer A Pre-Load Register - High Byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PLOAD_H[7:0]	R/W	Timer A pre-load data or PWM period data register – high byte	

Table 5-106 TMA_PLOAD_H register

TMA_L			**Page: 3 / Address: 0x9D**		**Timer A Counter Register - Low Byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMA_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_L[7:0]	R/W	Timer A counter register – low byte	

Table 5-107 TMA_L register

TMA_H			**Page: 3 / Address: 0x9E**		**Timer A Counter Register - High Byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMA_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_H[7:0]	R/W	Timer A counter register – high byte	

Table 5-108 TMA_H register

TMA_CAP_CTRL0			Page: 3 / Address: 0x9F		Timer A Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_CAPx_EN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMA_CAPx_EN[3:0]	R/W	Timer A capture mode enable control bit. All trigger sources are from external I/O. Following table is the trigger source mapping table. TMA_CAPx_EN — Mapping I/O TMA_CAP0_EN — P2[2] TMA_CAP1_EN — P2[1] TMA_CAP2_EN — P2[0] TMA_CAP3_EN — P2[3] 0: Disabled 1: Enabled	

Table 5-109 TMA_CAP_CTRL0 register

TMA_CAP_CTRL1			Page: 3 / Address: 0xA2		Timer A Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CAP3_EDGE[1:0]		TMA_CAP2_EDGE[1:0]		TMA_CAP1_EDGE[1:0]		TMA_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMA_CAP3_EDGE[7:6]	R/W	Timer A capture 3 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	
5:4	TMA_CAP2_EDGE[5:4]	R/W	Timer A capture 2 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	
3:2	TMA_CAP1_EDGE[3:2]	R/W	Timer A capture 1 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	
1:0	TMA_CAP0_EDGE[1:0]	R/W	Timer A capture 0 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	

Table 5-110 TMA_CAP_CTRL1 register

TMA_CAP_INTEN			Page: 3 / Address: 0xA4		Timer A Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_CAPx_INTEN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMA_CAPx_INTEN[3:0]	R/W	Timer A capture mode interrupt enable control bits. These are mapped to CAP0 ~ CAP3 respectively. 0: Disabled 1: Enabled	

Table 5-111 TMA_CAP_INTEN register

TMA_CAP_INTSTS			Page: 3 / Address: 0xA5		Timer A Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_CAPx_INTSTS[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMA_CAPx_INTSTS[3:0]	R/W	Timer A capture mode interrupt status register. These are mapped to CAP0 ~ CAP3 respectively. Read : 0: No capture triggered 1: Capture triggered Write : 0: Clears this bit 1: No effect	

Table 5-112 TMA_CAP_INTSTS register

TMA_PWM_CTRL0			Page: 3 / Address: 0xA6		Timer A PWM Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	DUTY_MODE	--	--	--	TMA_PWMx_EN			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	DUTY_MODE	R/W	Timer A PWM duty control selection bit. ***This bit is available when PWM operating in center alignment mode.*** 0: PWM duty is controlled by TMA_CCPx_L / TMA_CCPx_H 1: PWM duty is controlled by TMA_CCPx_L / TMA_CCPx_H / TMA_PWMx_L / TMA_PWMx_END_L / TMA_PWMx_END_H. In PWM rising edge , transition point is depended on TMA_CCPx_L / TMA_CCPx_H. Opposite, transition point is depended on TMA_PWMx_END_L / TMA_PWMx_END_H.	
6:4	--	R/W	Reserved	Read 0
[3:0]	TMA_PWMx_EN	R/W	Timer A PWM mode enable bits 0: Disabled	

Bit	Function	Type	Description	Condition
			1: Enabled	

Table 5-113 TMA_PWM_CTRL0 register

TMA_PWM_CTRL1			Page: 3 / Address: 0xA7		Timer A PWM Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	OVC_EN	DUTY_DIR_WR_EN	--	--	--	TMA_PWM23_MODE	--	TMA_PWM01_MODE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	OVC_EN	R/W	Over current break enable 0: Disabled 1: Enabled	
6	DUTY_DIR_WR_EN	R/W	PWM duty is updated immediately when CPU write data into PWM duty registers 0: Disabled 1: Enabled	
5:3	--	R/W	Reserved	
2	TMA_PWM23_MODE	R/W	Timer A PWM 2/3 operationg mode selection bit 0: Independent mode 1: Complementary mode	
1	--	R/W	Reserved	
0	TMA_PWM01_MODE	R/W	Timer A PWM 0/1 operationg mode selection bit 0: Independent mode 1: Complementary mode	

Table 5-114 TMA_PWM_CTRL1 register

TMA_PWM_CTRL2			Page: 3 / Address: 0xAA		Timer A PWM Control 2 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_PWMx_POL			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3	TMA_PWM3_POL	R/W	Timer A PWM3 polarity setting Independent mode: 0: PWM3 output low when PWM_cnt = TMA_CCP3 1: PWM3 output high when PWM_cnt = TMA_CCP3 Complementary mode: 0: PWM3 output high when PWM_cnt = TMA_CCP2 1: PWM3 output low when PWM_cnt = TMA_CCP2	
2	TMA_PWM2_POL	R/W	Timer A PWM2 polarity setting Independent mode: 0: PWM2 output low when PWM_cnt = TMA_CCP2 1: PWM2 output high when PWM_cnt = TMA_CCP2 Complementary mode:	

Bit	Function	Type	Description	Condition
			0: PWM2 output low when PWM_cnt = TMA_CCP2 1: PWM2 output high when PWM_cnt = TMA_CCP2	
1	TMA_PWM1_POL	R/W	Timer A PWM1 polarity setting Independent mode: 0: PWM1 output low when PWM_cnt = TMA_CCP1 1: PWM1 output high when PWM_cnt = TMA_CCP1 Complementary mode: 0: PWM1 output high when PWM_cnt = TMA_CCP0 1: PWM1 output low when PWM_cnt = TMA_CCP0	
0	TMA_PWM0_POL	R/W	Timer A PWM0 polarity setting Independent mode: 0: PWM0 output low when PWM_cnt = TMA_CCP0 1: PWM0 output high when PWM_cnt = TMA_CCP0 Complementary mode: 0: PWM0 output low when PWM_cnt = TMA_CCP0 1: PWM0 output high when PWM_cnt = TMA_CCP0	

Table 5-115 TMA_PWM_CTRL2 register

TMA_PWM_CTRL3			**Page: 3 / Address: 0xAB**		**Timer A PWM Control 3 Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_PWMx_SRC_CTR			
Default	0	0	0	0	1	1	1	1

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	TMA_PWMx_CTR_SRC	R/W	PWM output source control bit 0: PWM output is depended on PWMOVRD register 1: PWM output is depended on PWM time base	

Table 5-116 TMA_PWM_CTRL3 register

TMA_PWM_OVRD			**Page: 3 / Address: 0xAC**		**Timer A PWM Override Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_PWMx_OVRD[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	TMA_PWMx_OVRD[3:0]	R/W	PWM override control data 0: PWM output is 0 1: PWM output is 1	

Table 5-117 TMA_PWM_OVRD register

TMA_PWM_DTIME			**Page: 3 / Address: 0xAD**		**Timer A PWM Override Register**			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM_DTIME[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM_DTIME[7:0]	R/W	Timer A PWM dead time register	

Table 5-118 TMA_PWM_DTIME register

TMA_CCP0_L			Page: 3 / Address: 0xAE		Timer A Counter / Capture / PWM 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP0_L[7:0]	R/W	Timer A Counter / Capture / PWM 0 register – low byte	

Table 5-119 TMA_CCP0_L register

TMA_CCP0_H			Page: 3 / Address: 0xAF		Timer A Counter / Capture / PWM 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP0_H[7:0]	R/W	Timer A Counter / Capture / PWM 0 register – high byte	

Table 5-120 TMA_CCP0_H register

TMA_CCP1_L			Page: 3 / Address: 0xB2		Timer A Counter / Capture / PWM 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP1_L[7:0]	R/W	Timer A Counter / Capture / PWM 1 register – low byte	

Table 5-121 TMA_CCP1_L register

TMA_CCP1_H			Page: 3 / Address: 0xB3		Timer A Counter / Capture / PWM 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP1_H[7:0]	R/W	Timer A Counter / Capture / PWM 1 register – high byte	

Table 5-122 TMA_CCP1_H register

TMA_CCP2_L			Page: 3 / Address: 0xB4		Timer A Counter / Capture / PWM 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP2_L[7:0]	R/W	Timer A Counter / Capture / PWM 2 register – low byte	

Table 5-123 TMA_CCP2_L register

TMA_CCP2_H			Page: 3 / Address: 0xB5		Timer A Counter / Capture / PWM 2 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP2_H[7:0]	R/W	Timer A Counter / Capture / PWM 2 register – high byte	

Table 5-124 TMA_CCP2_H register

TMA_CCP3_L			Page: 3 / Address: 0xB6		Timer A Counter / Capture / PWM 3 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP3_L[7:0]	R/W	Timer A Counter / Capture / PWM 3 register – low byte	

Table 5-125 TMA_CCP3_L register

TMA_CCP3_H			Page: 3 / Address: 0xB7		Timer A Counter / Capture / PWM 3 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP3_H[7:0]	R/W	Timer A Counter / Capture / PWM 3 register – high byte	

Table 5-126 TMA_CCP3_H register

TMA_PWM0_END_L			Page: 3 / Address: 0xC4		Timer A PWM0 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM0_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM0_END_L[7:0]	R/W	Timer A PWM0 end duty register – low byte	

Table 5-127 TMA_PWM0_END_L register

TMA_ PWM0_END_H			Page: 3 / Address: 0xC5		Timer A PWM0 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM0_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM0_END_H[7:0]	R/W	Timer A PWM0 end duty register – high byte	

Table 5-128 TMA_PWM0_END_H register

TMA_PWM1_END_L			Page: 3 / Address: 0xC6		Timer A PWM1 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM1_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM1_END_L[7:0]	R/W	Timer A PWM1 end duty register – low byte	

Table 5-129 TMA_PWM1_END_L register

TMA_ PWM1_END_H			Page: 3 / Address: 0xC7		Timer A PWM1 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM1_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM1_END_H[7:0]	R/W	Timer A PWM1 end duty register – high byte	

Table 5-130 TMA_PWM1_END_H register

TMA_PWM2_END_L			Page: 3 / Address: 0xCA		Timer A PWM2 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM2_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM2_END_L[7:0]	R/W	Timer A PWM2 end duty register – low byte	

Table 5-131 TMA_PWM2_END_L register

TMA_ PWM2_END_H			Page: 3 / Address: 0xCB		Timer A PWM2 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM2_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM2_END_H[7:0]	R/W	Timer A PWM2 end duty register – high byte	

Table 5-132 TMA_PWM2_END_H register

TMA_PWM3_END_L			Page: 3 / Address: 0xCC		Timer A PWM3 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM3_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM3_END_L[7:0]	R/W	Timer A PWM3 end duty register – low byte	

Table 5-133 TMA_PWM3_END_L register

TMA_ PWM3_END_H			**Page: 3 / Address: 0xCD**		**Timer A PWM3 End Duty Register – high byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM3_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM3_END_H[7:0]	R/W	Timer A PWM3 end duty register – high byte	

Table 5-134 TMA_PWM3_END_H register

5.9.4. Timer B

The Timer B, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture/PWM feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

5.9.4.1. Timer / Counter mode

In timer / counter function, that have up to 8 clock sources can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The Figure 5-28 shows the block diagram of counter / timer function for Timer B. When Timer B rolls over from pre-load data (TMB_PLOAD_H/L) to 0, not only TMB_INTF is set, but also Timer B registers is loaded with the 16-bit value from TMB_PLOAD_H/L register. Required TMB_PLOAD_H/L value can be preset by software.

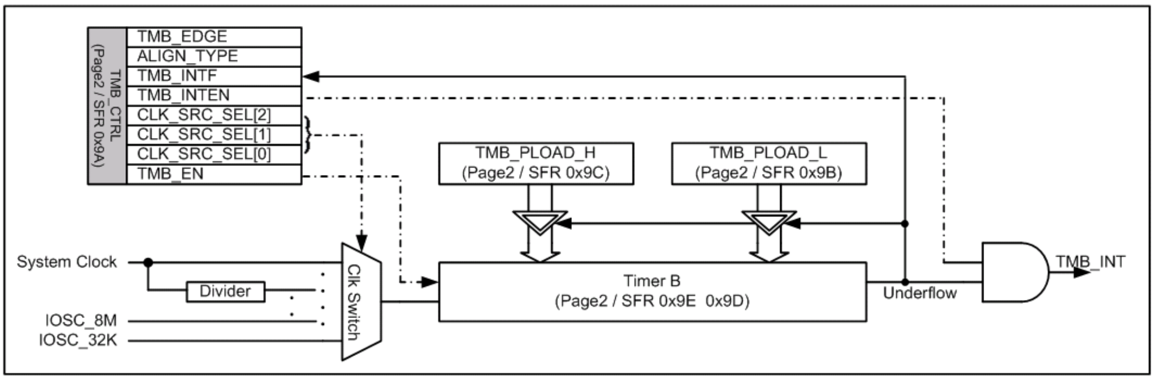


Figure 5-28 The block diagram of counter / timer function for Timer B

5.9.4.2. Capture function

Each of capture registers can be used to latch the current 16-bit value of the Timer B registers (TMB_H and TMB_L) when an external event is triggered. Figure 5-29 shows functional diagrams of the Timer B capture function.

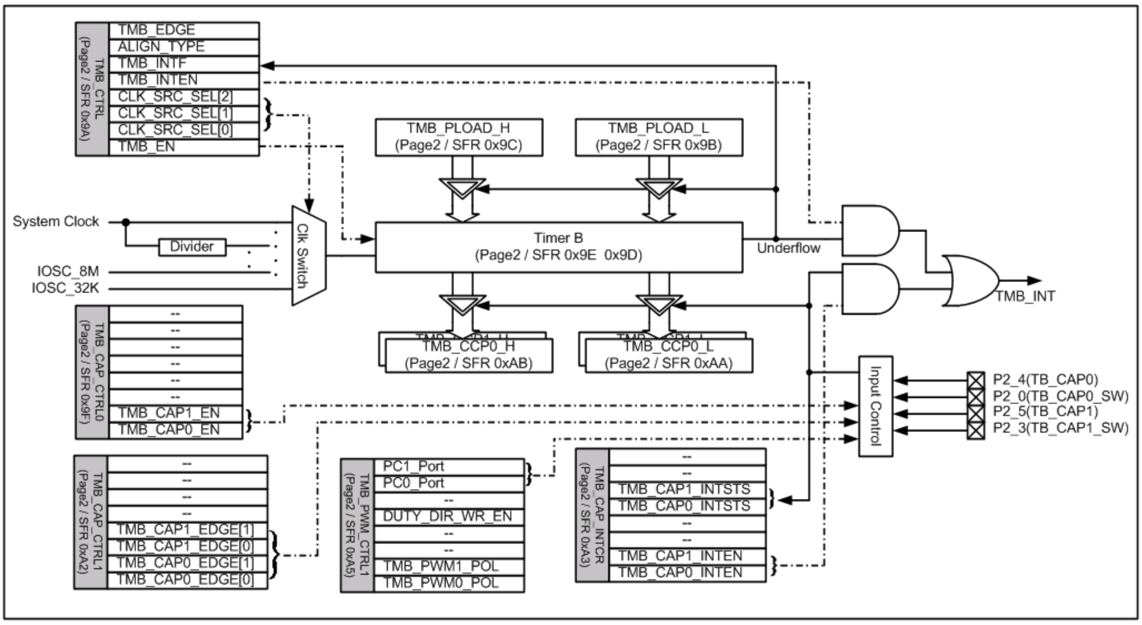


Figure 5-29 The block diagram of Timer B capture mode

5.9.4.3. PWM function

The Timer B consists of 2 sets PWM function. When the TMB_PWMx_EN is enabled, the PWM output will toggle at the TMB_H/L are lesser or greater than TMB_CCPx_H/L value. About Timer count policy, there are two options can be choice between edge and center alignment. In edge alignment, the counter decrease counter value per clock cycle. Hardware will auto re-load TMB_PLOAD_H/L value to counter when counter is underflow. In center of alignment, the counter is executing down count first and executing up-count next. There are two output modes of PWM output pin: independent and complement mode. In each mode, user can change output polarity with TMB_PWM_CTRL1 randomly. Figure 5-30 shows functional diagrams of the Timer B PWM function, and Figure 5-31 to Figure 5-36 are PWM operating waveform.

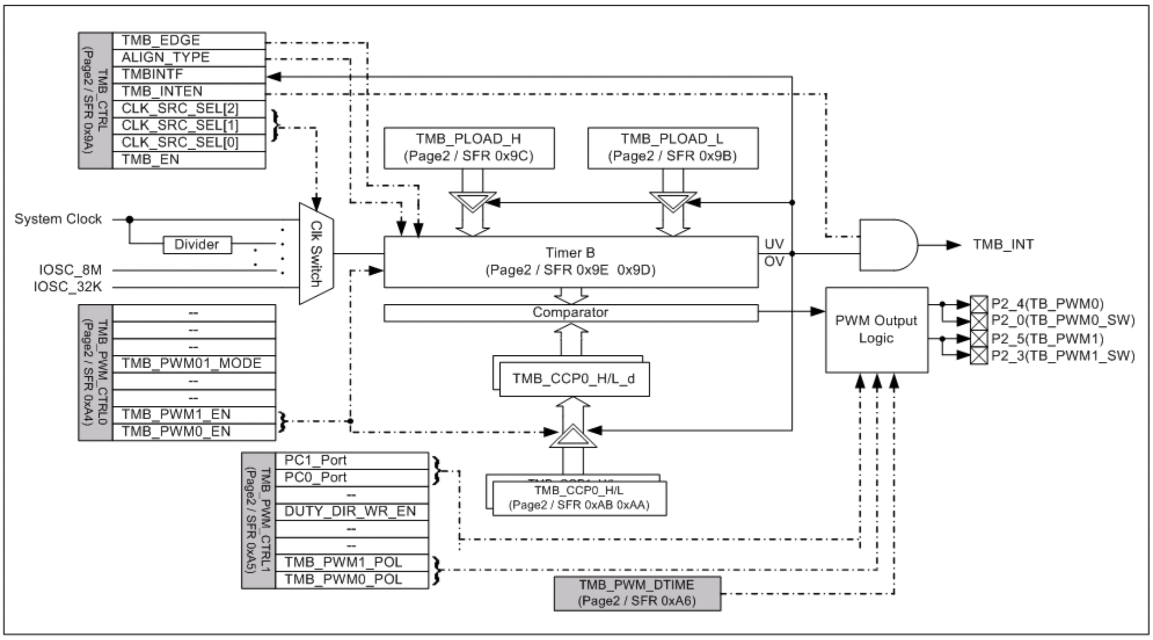


Figure 5-30 The block diagram of Timer B PWM mode

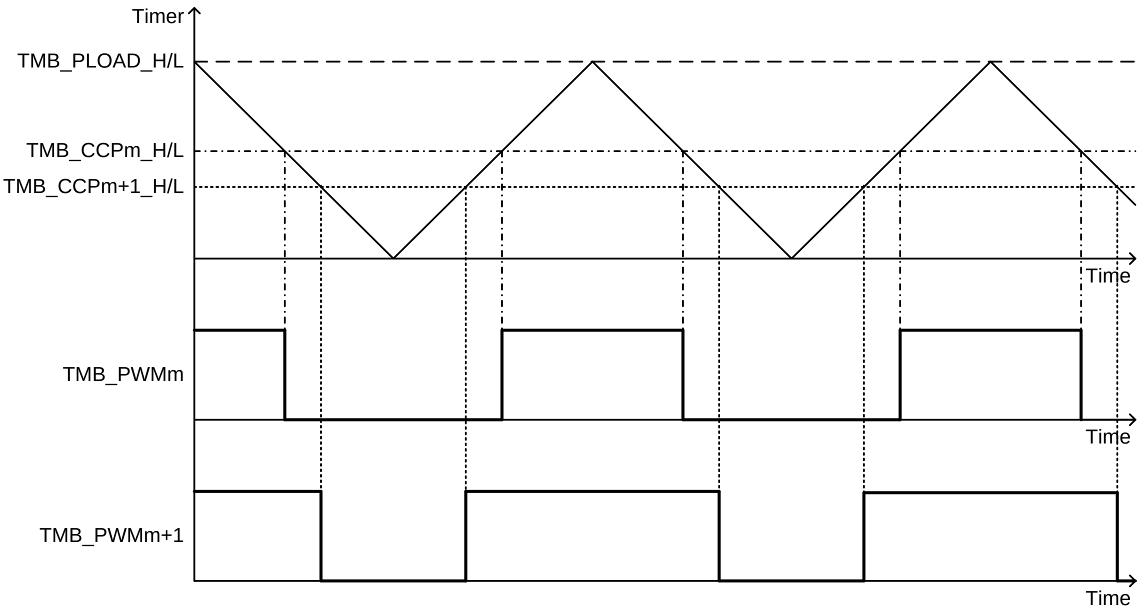


Figure 5-31 The waveform of Timer B PWM without dead time (ALIGN_TYPE: 1 / DUTY_MODE: 0 / TMB_PWMx_MODE: 0 ; m=0)

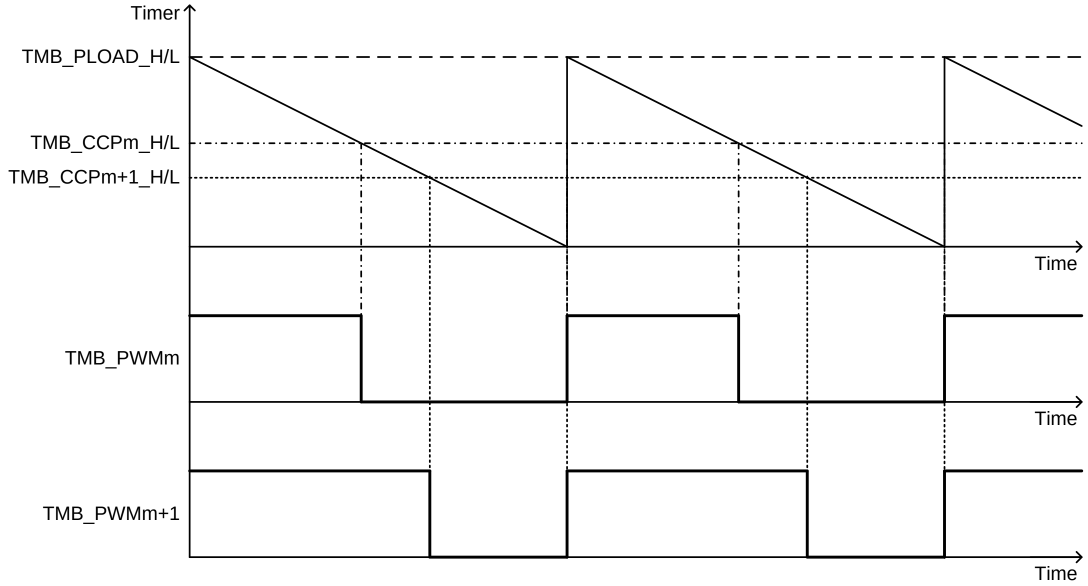


Figure 5-32 The waveform of Timer B PWM without dead time (ALIGN_TYPE: 0 / DUTY_MODE: 0 / TMB_PWMx_MODE: 0 ; m=0)

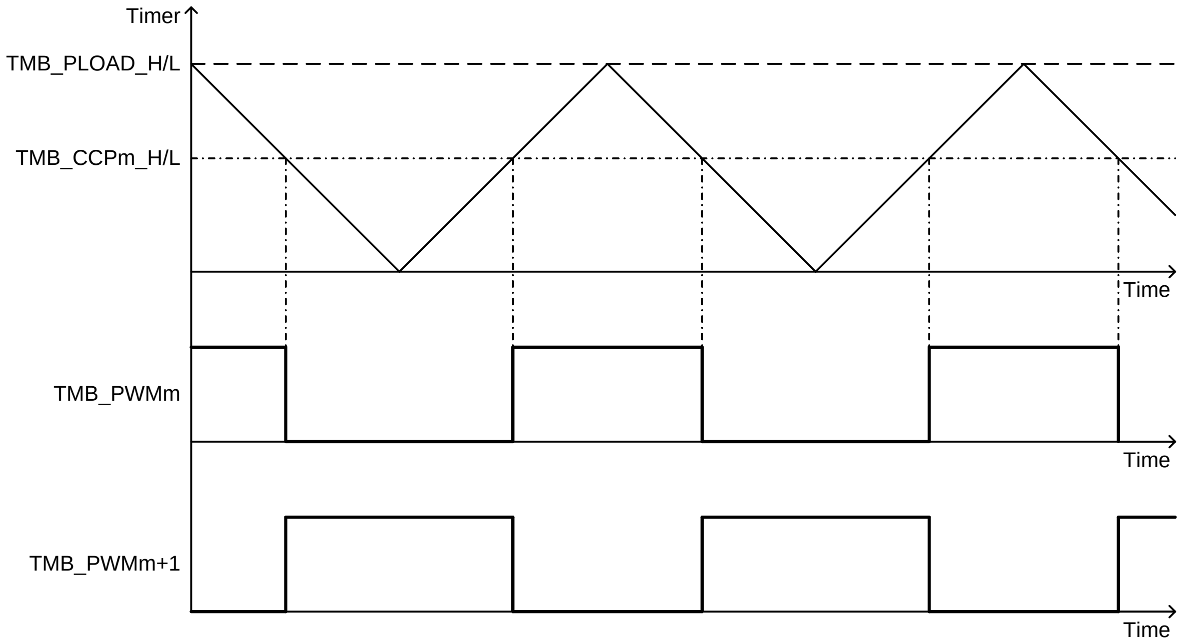


Figure 5-33 The waveform of Timer B PWM without dead time (ALIGN_TYPE: 1 / DUTY_MODE: 0 / TMB_PWMx_MODE: 1 ; m=0)

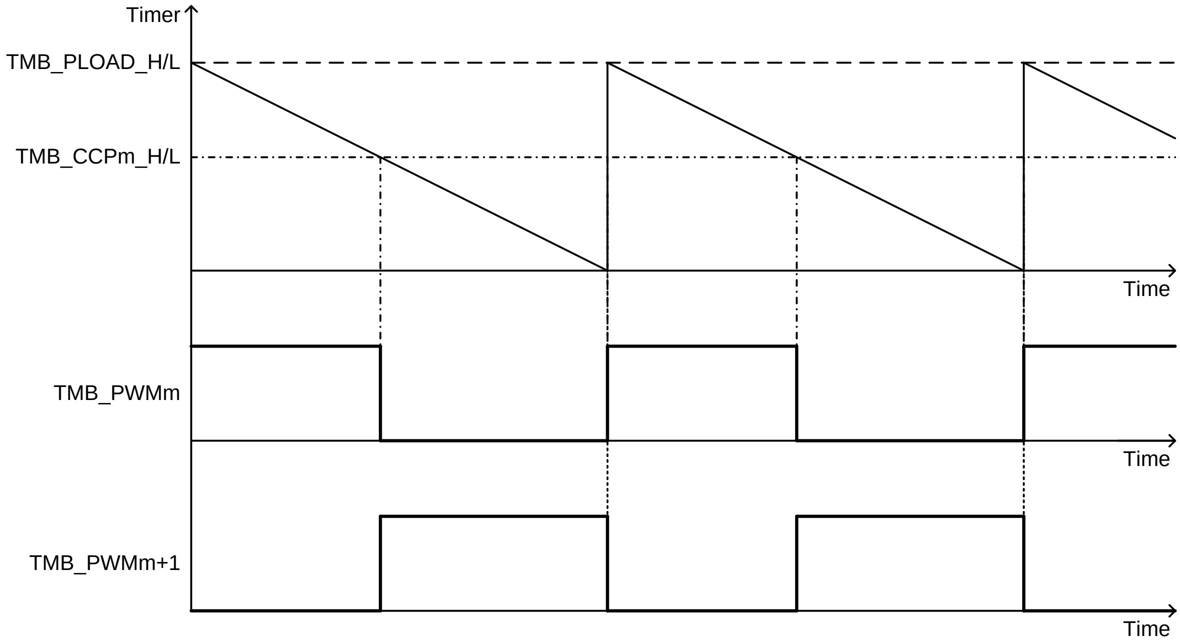


Figure 5-34 The waveform of Timer B PWM without dead time (ALIGN_TYPE: 0 / DUTY_MODE: 0 / TMB_PWMx_MODE: 1 ; m=0)

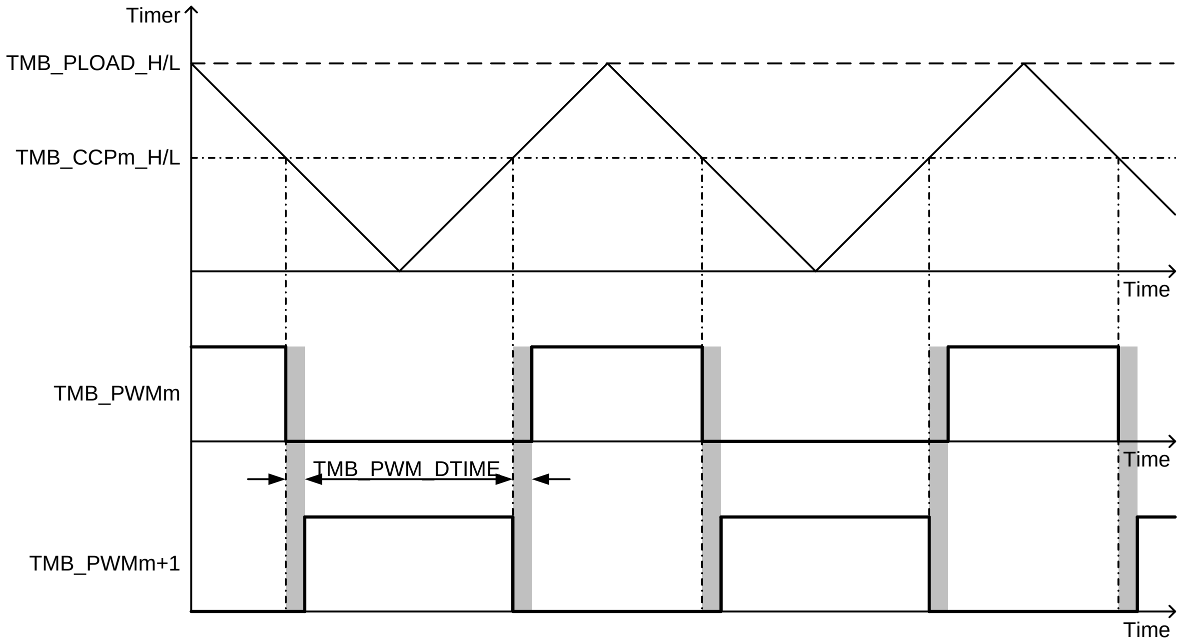


Figure 5-35 The waveform of Timer B PWM with dead time (ALIGN_TYPE: 1 / DUTY_MODE: 0 / TMB_PWMx_MODE: 1 ; m=0)

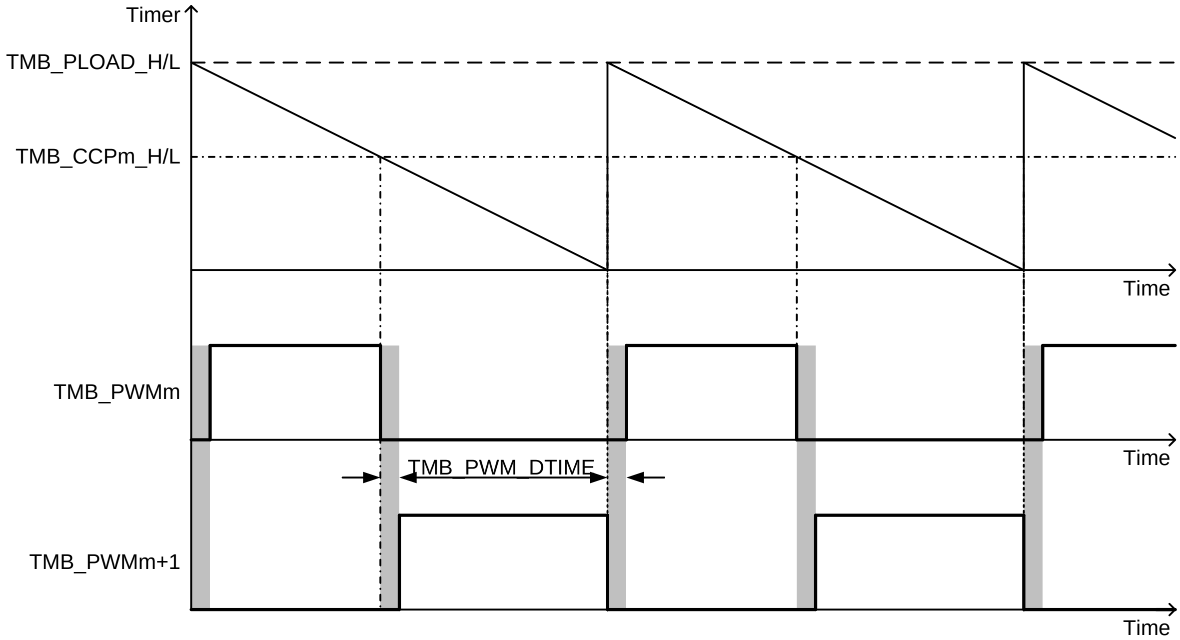


Figure 5-36 The waveform of Timer B PWM with dead time (ALIGN_TYPE: 0 / DUTY_MODE: 0 / TMB_PWMx_MODE: 1 ; m=0)

5.9.4.4. Timer B Related Registers

TMB_CTRL			Page: 2 / Address: 0x9A		Timer B Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMB_EDGE	R	Timer B up/down count edge indication. 0: Falling edge 1: Rising edge	
6	ALIGN_TYPE	R/W	0: Edge alignment 1: Center alignment	
5	TMB_INTF	R/W	Timer B interrupt flag Read: 0: Idle / busy 1: Timer B interrupt trigger Write : 0: Clears this bit 1: No effect	
4	TMB_INTEN	R/W	Timer B interrupt enable control bit 0: Disabled 1: Enabled	
3:1	CLK_SRC_SEL	R/W	Timer B input clock source selection control bit CLK_SRC_SEL[2:0] : Clock Source 000 : System clock 001 : System clock / 2 010 : System clock / 4 011 : System clock / 8 100 : System clock / 16 101 : System clock / 32 110 : IOSC_8M 111 : 32K (IOSC_32K) Note: when CLK_SRC_SEL select IOSC8M, the system clock must faster more 2 times than IOSC8M.	
0	TMB_EN	R/W	Timer B enable control bit. 0: Disabled 1: Enabled	

Table 5-135 TMB_CTRL register

TMB_PLOAD_L			Page: 2 / Address: 0x9B		Timer B Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PLOAD_L[7:0]	R/W	Timer B pre-load data or PWM period data register – low byte	

Table 5-136 TMB_PLOAD_L register

TMB_PLOAD_H			Page: 2 / Address: 0x9C		Timer B Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PLOAD_H[7:0]	R/W	Timer B pre-load data or PWM period data register – high byte	

Table 5-137 TMB_PLOAD_H register

TMB_L			Page: 2 / Address: 0x9D		Timer B Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_L[7:0]	R/W	Timer B counter register – low byte	

Table 5-138 TMB_L register

TMB_H			Page: 2 / Address: 0x9E		Timer B Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_H[7:0]	R/W	Timer B counter register – high byte	

Table 5-139 TMB_H register

TMB_CAP_CTRL0			Page: 2 / Address: 0x9F		Timer B Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	TMB_CAPx_EN[1:0]	
Default	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:2</td><td>--</td><td>R/W</td><td>Reserved</td><td>Read 0</td></tr>
<tr><td>1:0</td><td>TMB_CAPx_EN[1:0]</td><td>R/W</td><td>Timer B capture mode enable control bit. All of the trigger source are from external I/O. Following table is the trigger source mapping table.
<table><tr><td>TMB_CAPx_EN</td><td>Mapping I/O</td></tr><tr><td>TMB_CAP0_EN</td><td>P2[4] or P2[0]</td></tr><tr><td>TMB_CAP1_EN</td><td>P2[5] or P2[3]</td></tr></table>0: Disabled
1: Enabled</td><td></td></tr>
</table>

Table 5-140 TMB_CAP_CTRL0 register

TMB_CAP_CTRL1			Page: 2 / Address: 0xA2		Timer B Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMB_CAP1_EDGE[1:0]		TMB_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:2	TMB_CAP1_EDGE[1:2]	R/W	Timer B capture 1 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	
1:0	TMB_CAP0_EDGE[1:0]	R/W	Timer B capture 0 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	

Table 5-141 TMB_CAP_CTRL1 register

TMB_CAP_INTCTRL			Page: 2 / Address: 0xA3		Timer B Capture Mode Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMB_CAP_INTSTS[1:0]		--	--	TMB_CAP_INTEN[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	Read 0
5:4	TMB_CAP_INTSTS[1:0]	R/W	Timer B capture mode trigger flag. These are mapped to CAP0 ~ CAP1 respectively. Read : 0: No capture signal triggered 1: Capture signal triggered Write : 0: Clears this bit 1: No effect	
3:2	--	R/W	Reserved	Read 0
1:0	TMB_CAP_INTEN[1:0]	R/W	Timer B capture mode interrupt enable control bits. These are mapped to CAP0 ~ CAP1 respectively. 0: Disabled 1: Enabled	

Table 5-142 TMB_CAP_INTCTRL registers

TMB_PWM_CTRL0			Page: 2 / Address: 0xA4		Timer B PWM Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	TMB_PWM01_MODE	--	--	TMB_PWMx_EN[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	TMB_PWM01_MODE	R/W	Timer B PWM 0/1 operationg mode selection bit 0: Independent mode 1: Complementary mode	
3:2	--	R/W	Reserved	
1:0	TMB_PWMx_EN[1:0]	R/W	Timer B PWM mode enable bits 0: Disabled 1: Enabled	

Table 5-143 TMB_PWM_CTRL0 register

TMB_PWM_CTRL1			Page: 2 / Address: 0xA5		Timer B PWM Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	PC1_Port	PC0_Port	--	DUTY_DIR_ WR_EN	--	--	TMB_PWMx_POL[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	PC1_Port	R/W	PWM / Capture 1 port select 0: P25 as PWM1 / Capture 1 function port 1: P23 as PWM1 / Capture 1 function port	
6	PC0_Port	R/W	PWM / Capture 0 port select 0: P24 as PWM0 / Capture 0 function port 1: P20 as PWM0 / Capture 0 function port	
5	--	R/W	Reserved	
4	DUTY_DIR_WR_EN	R/W	PWM duty is updated immediately when CPU writes data into PWM duty registers 0: Disabled 1: Enabled	
3	--	R/W	Reserved	
2	--	R/W	Reserved	
1	TMB_PWM1_POL	R/W	Timer B PWM1 polarity setting Independent mode: 0: PWM1 output low when PWM_cnt = TMB_CCP1 1: PWM1 output high when PWM_cnt = TMB_CCP1 Complementary mode: 0: PWM1 output high when PWM_cnt = TMB_CCP0 1: PWM1 output low when PWM_cnt = TMB_CCP0	
0	TMB_PWM0_POL	R/W	Timer B PWM0 polarity setting Independent mode: 0: PWM0 output low when PWM_cnt = TMB_CCP0 1: PWM0 output high when PWM_cnt = TMB_CCP0 Complementary mode: 0: PWM0 output low when PWM_cnt = TMB_CCP0 1: PWM0 output high when PWM_cnt = TMB_CCP0	

Table 5-144 TMB_PWM_CTRL1 register

TMB_PWM_DTIME			Page: 2 / Address: 0xA6		Timer B PWM Dead Time Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_PWM_DTIME[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PWM_DTIME[7:0]	R/W	Timer B PWM dead time register	

Table 5-145 TMB_PWM_DTIME register

TMB_CCP0_L			Page: 2 / Address: 0xAA		Timer B Counter / Capture / PWM 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP0_L[7:0]	R/W	Timer B Counter / Capture / PWM 0 register – low byte	

Table 5-146 TMB_CCP0_L register

TMB_CCP0_H			Page: 2 / Address: 0xAB		Timer B Counter / Capture / PWM 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP0_H[7:0]	R/W	Timer B Counter / Capture / PWM 0 register – high byte	

Table 5-147 TMB_CCP0_H register

TMB_CCP1_L			Page: 2 / Address: 0xAC		Timer B Counter / Capture / PWM 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP1_L[7:0]	R/W	Timer B Counter / Capture / PWM 1 register – low byte	

Table 5-148 TMB_CCP1_L register

TMB_CCP1_H			Page: 2 / Address: 0xAD		Timer B Counter / Capture / PWM 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP1_H[7:0]	R/W	Timer B Counter / Capture / PWM 1 register – high byte	

Table 5-149 TMA_CCP1_H register

5.9.5. Timer C

The Timer C, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture feature is one of the most powerful peripheral units of the core. It can be used for all kinds of event capturing.

5.9.5.1. Timer / Counter mode

In timer / counter function, that have up to 7 clock source can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The Figure 5-37 shows the block diagram of counter / timer function for Timer C. When Timer C rolls over from pre-load data (TMC_PLOAD_H/L) to 0, not only TMC_INTF is set but also Timer C registers is loaded with the 16-bit value from TMC_PLOAD_H/L register. Required TMC_PLOAD_H/L value can be preset by software.

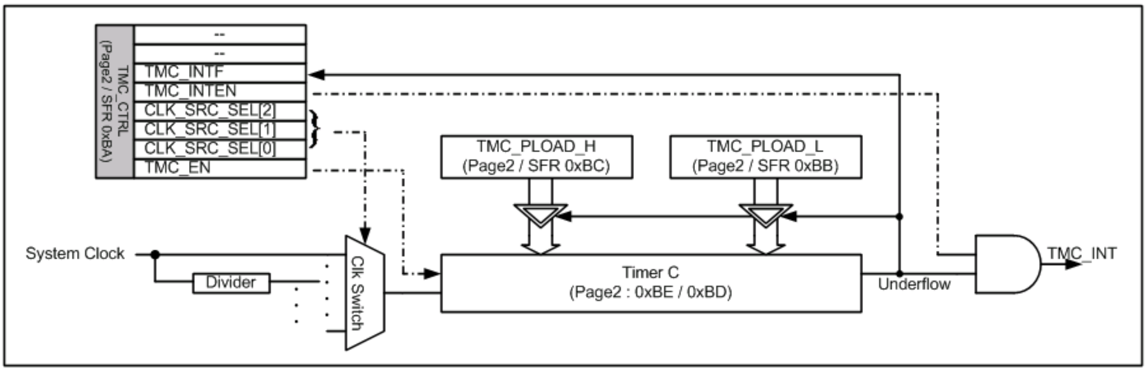


Figure 5-37 The block diagram of counter / timer function for Timer C

5.9.5.2. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer C registers (TMC_H and TMC_L) when an external event is triggered. Figure 5-38 shows functional diagrams of the Timer C capture function.

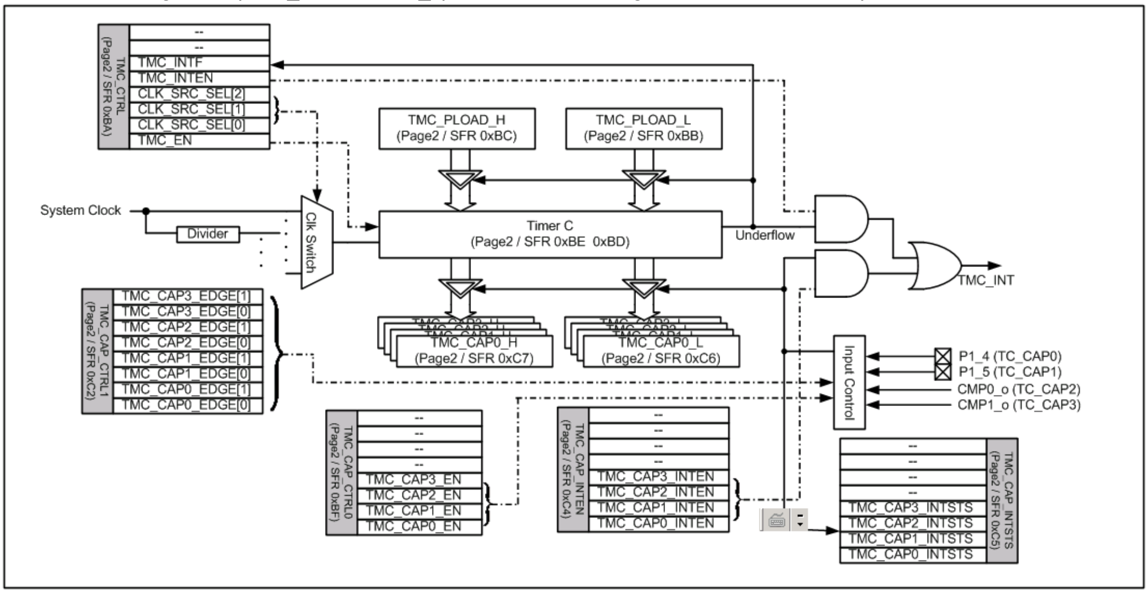


Figure 5-38 The block diagram of Timer C capture mode

5.9.5.3. Timer C Related Registers

TMC_CTRL			Page: 2 / Address: 0xBA		Timer C Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	TMC_INTF	R/W	Timer C interrupt flag Read: 0: Idle / busy 1: Timer C interrupt trigger Write: 0: Clears this bit 1: No effect	
4	TMC_INTEN	R/W	Timer C interrupt enable control bit 0: Disabled 1: Enabled	
3:1	CLK_SRC_SEL	R/W	Timer C input clock source selection control bit CLK_SRC_SEL[2:0] – Clock Source 000 – System clock 001 – System clock / 2 010 – System clock / 4 011 – System clock / 128 100 – System clock / 256 101 – System clock / 512 110 – System clock / 1024 111 – Prohibit	
0	TMC_EN	R/W	Timer C enable control bit. 0: Disabled 1: Enabled	

Table 5-150 TMC_CTRL register

TMC_PLOAD_L			Page: 2 / Address: 0xBB		Timer C Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_PLOAD_L[7:0]	R/W	Timer C pre-load data or PWM period data register – low byte	

Table 5-151 TMC_PLOAD_L register

TMC_PLOAD_H			Page: 2 / Address: 0xBC		Timer C Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_PLOAD_H[7:0]	R/W	Timer C pre-load data or PWM period data register – high byte	

Table 5-152 TMC_PLOAD_H register

TMC_L			Page: 2 / Address: 0xBD		Timer C Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_L[7:0]	R/W	Timer C counter register – low byte	

Table 5-153 TMC_L register

TMC_H			Page: 2 / Address: 0xBE		Timer C Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_H[7:0]	R/W	Timer C counter register – high byte	

Table 5-154 TMB_H register

TMC_CAP_CTRL0			Page: 2 / Address: 0xBF		Timer C Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMC_CAPx_EN[2:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMC_CAPx_EN[2:0]	R/W	Timer C capture mode enable control bit. All trigger sources are from external I/O. Following table is the trigger source mapping table. TMC_CAPx_EN: Mapping I/O TMC_CAP0_EN: P1[4] TMC_CAP1_EN: P1[5] TMC_CAP2_EN: CMP0_o TMC_CAP3_EN: CMP1_o 0: Disabled 1: Enabled	

Table 5-155 TMC_CAP_CTRL0 register

TMC_CAP_CTRL1			Page: 2 / Address: 0xC2		Timer C Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_EDGE[1:0]		TMC_CAP2_EDGE[1:0]		TMC_CAP1_EDGE[1:0]		TMC_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMC_CAP3_EDGE[7:6]	R/W	Timer C capture 3 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	Read 0
5:4	TMC_CAP2_EDGE[5:4]	R/W	Timer C capture 2 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	
3:2	TMC_CAP1_EDGE[3:2]	R/W	Timer C capture 1 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	
1:0	TMC_CAP0_EDGE[1:0]	R/W	Timer C capture 0 sample edge selection bit 00: Falling edge 01: Rising edge 1x: Both edges	

Table 5-156 TMC_CAP_CTRL1 register

TMC_CAP_INTEN			**Page: 2 / Address: 0xC4**		**Timer C Capture Mode Interrupt Enable Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMC_CAPx_INTEN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMC_CAPx_INTEN[3:0]	R/W	Timer C capture mode interrupt enable control bits. These are mapped to CAP0 ~ CAP3 respectively. 0: Disabled 1: Enabled	

Table 5-157 TMC_CAP_INTEN register

TMC_CAP_INTSTS			**Page: 2 / Address: 0xC5**		**Timer C Capture Mode Interrupt Status Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMC_CAPx_INTSTS[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	Read 0
3:0	TMC_CAPx_INTSTS[3:0]	R/W	Timer C capture mode interrupt status register. These are mapped to CAP0 ~ CAP3 respectively. Read : 0: No capture triggered 1: Capture triggered Write : 0: Clears this bit 1: No effect	

Table 5-158 TMC_CAP_INTSTS register

TMC_CAP0_L			Page: 2 / Address: 0xC6		Timer C Capture 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP0_L[7:0]	R/W	Timer C Capture 0 register – low byte	

Table 5-159 TMC_CAP0_L register

TMC_CAP0_H			Page: 2 / Address: 0xC7		Timer C Capture 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP0_H[7:0]	R/W	Timer C Capture 0 register – high byte	

Table 5-160 TMC_CAP0_H register

TMC_CAP1_L			Page: 2 / Address: 0xCA		Timer C Capture 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP1_L[7:0]	R/W	Timer C Capture 1 register – low byte	

Table 5-161 TMC_CAP1_L register

TMC_CAP1_H			Page: 2 / Address: 0xCB		Timer C Capture 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP1_H[7:0]	R/W	Timer C Capture 1 register – high byte	

Table 5-162 TMC_CAP1_H register

TMC_CAP2_L			Page: 2 / Address: 0xCC		Timer C Capture 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP2_L[7:0]	R/W	Timer C Capture 2 register – low byte	

Table 5-163 TMC_CAP2_L register

TMC_CAP2_H			**Page: 2 / Address: 0xCD**		**Timer C Capture 2 Register – high byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP2_H[7:0]	R/W	Timer C Capture 2 register – high byte	

Table 5-164 TMC_CAP2_H register

TMC_CAP3_L			**Page: 2 / Address: 0xCE**		**Timer C Capture 3 Register – low byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP3_L[7:0]	R/W	Timer C Capture 3 register – low byte	

Table 5-165 TMC_CAP3_L register

TMC_CAP3_H			**Page: 2 / Address: 0xCF**		**Timer C Capture3 Register – high byte**			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP3_H[7:0]	R/W	Timer C Capture 3 register – high byte	

Table 5-166 TMC_CAP3_H register

5.10. UART0

UART0 has the same functionality as a standard 8051 UART. The serial port is full duplex, meaning it can transmit and receive concurrently. It is reception with double-buffer, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. Figure 5-39 shows the block diagram of UART module. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM02 set and ignoring the incoming data.

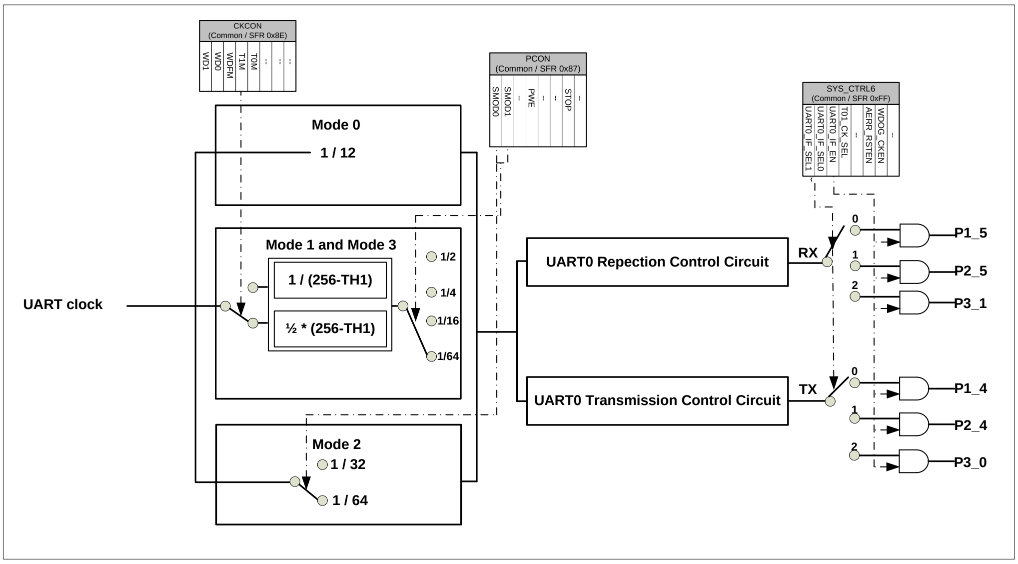


Figure 5-39 The block diagram of UART module

5.10.1. UART0: Mode 0(Synchronous Shift register)

This mode is used as shift register IO control, and not for real communication application. The baud rate is fixed at 1/12 of the system clock frequency and TX output is a shift clock. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0 =0 and REN0 =1. Figure 5-40 shows the timing diagram of UART0 transmission mode 0.

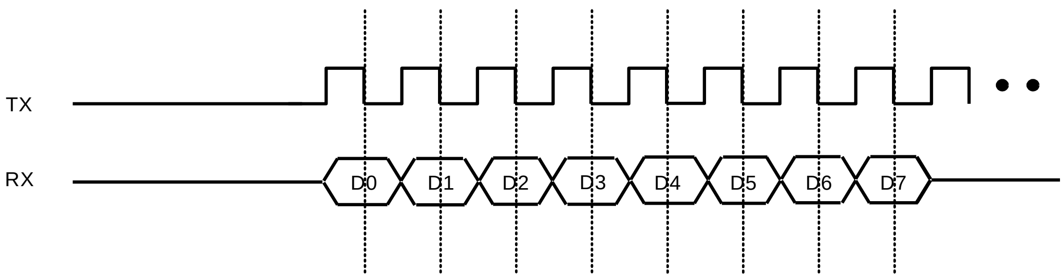


Figure 5-40 The timing diagram of UART0 transmission mode 0

5.10.2. UART0: Mode 1(8-Bit UART, Variable Baud Rate, Timer1 Clock Source)

In mode 1, TX serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receiving, a start bit synchronizes the reception, In UART0 function, 8 data bits are available by reading SBUF0 and stop bit sets the flag RB08 in the SFR SCON0. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5-41 shows the format of UART0 transmission mode 1.

Figure 5-41 The format of UART0 transmission mode 1

5.10.3. UART0: Mode 2(9-Bit UART, Fixed Baud Rate)

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of system clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9^{th} bit, and a stop bit (1). The 9^{th} bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0/1 is output as the 9th bit, and at receive, the 9th bit affects RB08 in SCON0/1. Figure 5-42 shows the format of UART0 transmission mode 2.

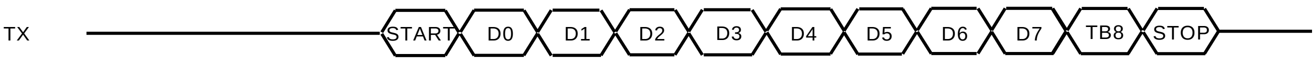


Figure 5-42 The format of UART0 transmission mode 2

5.10.4. UART0: Mode 3(9-Bit UART, Variable Baud Rate, Timer1 Clock Source)

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0/1 =1 data receiving is enabled. The baud rate is variable and depends from Timer 1 mode. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5-43 shows the format of UART0 transmission mode 3.

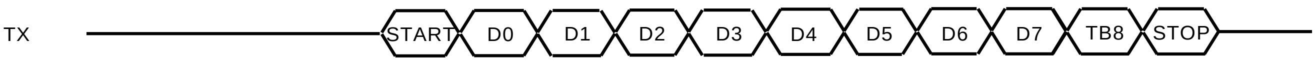


Figure 5-43 The format of UART0 transmission mode 3

5.10.5. UART0 Related Registers

The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8).
The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data written into SBUF0 sets this data in UART0 output register and starts a transmission. A data read from SBUF0, reads data from the UART0 receive register.

SBUF0			**Common/Address: 0x99**		**UART0 Buffer Register**			
Bit	7	6	5	4	3	2	1	0
Function	SBUF0[7:0]							
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	SBUF0	R/W	UART 0 buffer	

Table 5-167 SBUF0 register

SCON0			**Common/Address: 0x98**		**UART0 Configuration Register**			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:6	SM0[1:0]	R/W	Mode and baud rate setting which described as below table	
5	SM02	R/W	Enables a multiprocessor communication feature	

Bit	Function	Type	Description	Condition
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0 this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-168 SCON0 register

PCON			Common /Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: Disables FLASH write activity during MOVX instruction 1: Enables FLASH write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-169 PCON register

SYS_CTRL6			Common / Address: 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL		UART0_IF_EN	T01_CK_SEL	--	ADDR_RSTEN	WDOG_CKEN	--
Default	0	0	0	0	0	0	0	0
Key Code	0x8F / 0x32 / 0x50							

Bit	Function	Type	Description	Condition
7:6	UART_IF_SEL[1:0]	R/W	UART0 interface select 00: TX is P1_4 , RX is P1_5 (default) 01: TX is P2_4 , RX is P2_5 10: TX is P3_0 , RX is P3_1 11: Reserved	
5	UART0_IF_EN	R/W	UART0 interface enable signal. 0: Disabled 1: Enabled	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal. This bit is used combining with T0M/T1M of CKCON(0x8E). T0M /T1M | T01_CK_SEL | Timer0/1 Clock	

Bit	Function	Type	Description	Condition
			0 | 0 | System Clock / 8 0 | 1 | System Clock / 2 1 | 0 | System Clock / 4 1 | 1 | System Clock / 1	
3	--	R/W	Reserved	
2	ADDR_RSTEN	R/W	FLASH address over range reset enable 0: Disabled 1: Enabled	
1	WDOG_CKEN	R/W	Watchdog controller clock enable control bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-170 The SYS_CTRL6 register

CKCON			Common/Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0: WD[1:0] | Timeout 00 | 128ms 01 | 256ms 10 | 512ms 11 | 1024ms If WDFM=1: WD[1:0] | Timeout 00 | 8ms 01 | 16ms 10 | 32ms 11 | 64ms	
5	WDFM	R/W	Watchdog fast mode selection bit 0: watchdog fast mode is disabled 1: watchdog fast mode is enabled	
4	T1M	R/W	Timer 1 clock source selection signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T1M | T01_CK_SEL | Timer1 Clock 0 | 0 | System Clock / 8 0 | 1 | System Clock / 2 1 | 0 | System Clock / 4 1 | 1 | System Clock / 1	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>3</td><td>T0M</td><td>R/W</td><td>Timer 0 clock source selection signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table>
<tr><td>T0M</td><td>T01_CK_SEL</td><td>Timer0 Clock</td></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>2:0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-171 CKCON register

SM00	SM01	Mode	Function	Baud rate
0	0	0	Shift register	SYSCLK/12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	SYSCLK/64(SMOD0=0) SYSCLK/32(SMOD0=1)
1	1	3	9-bit UART	variable

Table 5-172 UART mode select table

- variable: in Mode1 and Mode 3(T1M=0)

SMOD1	SMOD0	Baud rate
0	0	T1ov/64(T1ov=SYSCLK/(256-TH1))
0	1	T1ov/16(T1ov=SYSCLK/(256-TH1))
1	0	T1ov/4(T1ov=SYSCLK/(256-TH1))
1	1	T1ov/2(T1ov=SYSCLK/(256-TH1))

IE			Common / Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	ETC	ETB	ES0	ET1	EADC	ET0	ETA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	ETC	R/W	Enable Timer C interrupt	
5	ETB	R/W	Enable Timer B interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EADC	R/W	Enable ADC interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	
0	ETA	R/W	Enable Timer A interrupt	

Table 5-173 IE register

IP			Common / Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	PTC	PTB	PS0	PT1	PADC	PT0	PTA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	PTC	R/W	Timer C interrupt priority level control (1: high level)	
5	PTB	R/W	Timer B interrupt priority level control (1: high level)	
4	PS0	R/W	UART0 interrupt priority level control (1: high level)	
3	PT1	R/W	Timer 1 interrupt priority level control (1: high level)	
2	PADC	R/W	ADC0/1 interrupt priority level control (1: high level)	
1	PT0	R/W	Timer 0 interrupt priority level control (1: high level)	
0	PTA	R/W	Timer A interrupt priority level control (1: high level)	

Table 5-174 IP register

5.11. SPI

A Serial Peripheral Interface (SPI) controller is built in GPM8F3331B to facilitate communicating with other devices and components. The SPI controller includes four master modes and one slaver mode. There are four control signals on SPI including SPI_CSB, SPI_CLK, SPI_TX, and SPI_RX, these four signals are shared with P3[3:0]. While SPI module is enabled by corresponding control bit, these four pins cannot be GPIOs. In other words, any setting on corresponding GPIO control register will have no effect. The SPI provides following features.

- ❑ Programmable phase and polarity of master clock
- ❑ Programmable master SPI_CLK clock frequency

In master mode, the shifting clock (SPI_CLK) is generated by SPI block. There are two control bits to control the clock phase and polarity. The transmission starts immediately after SPI_START is set(SPI_CTRL[0]=1, Page0 / 0x9A). The SPI shifts the 8-bit data from MSB to LSB through the SPI_TX pin during 8 SPI_CLK cycles. Programmer can read SPI data from SPI_RXD control register. The following four diagrams depict the timing scheme on SPI master mode for different operation types (polarity control bit equals “1” or “0”, phase control bit equals “1” or “0”). The related registers are SPI_CTRL register, SPI_STS register, SPI_TXD register and SPI_RXD registers which are tabled as Table 5-175 to Table 5-178.

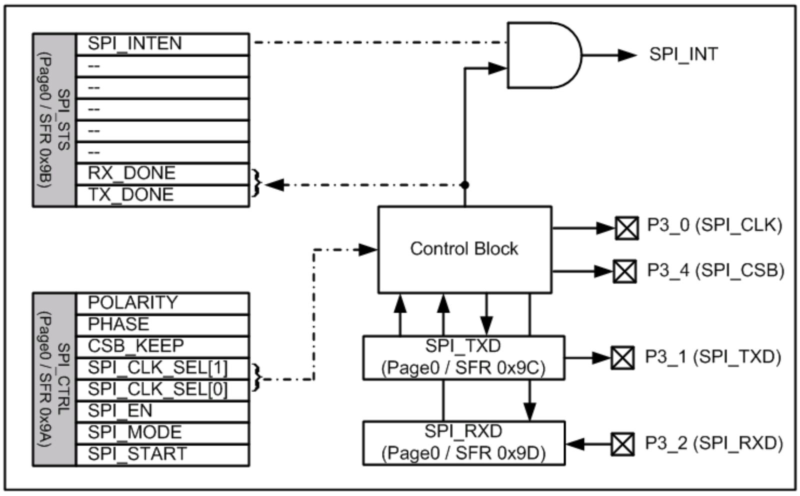


Figure 5-44 The block diagram of SPI controller

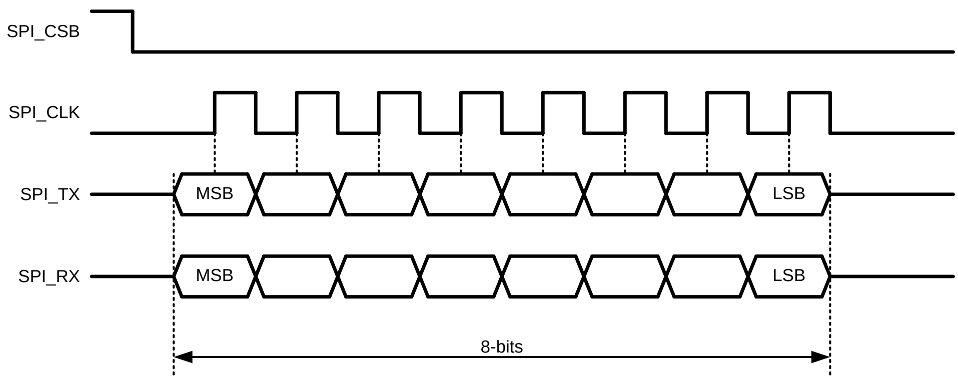


Figure 5-45 Master / Slaver Mode, POLARITY=0, PHASE=0

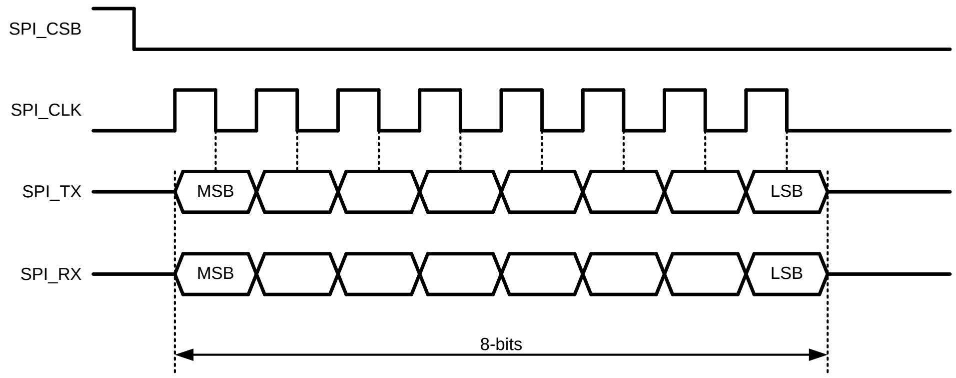


Figure 5-46 Master Mode, POLARITY=0, PHASE=1

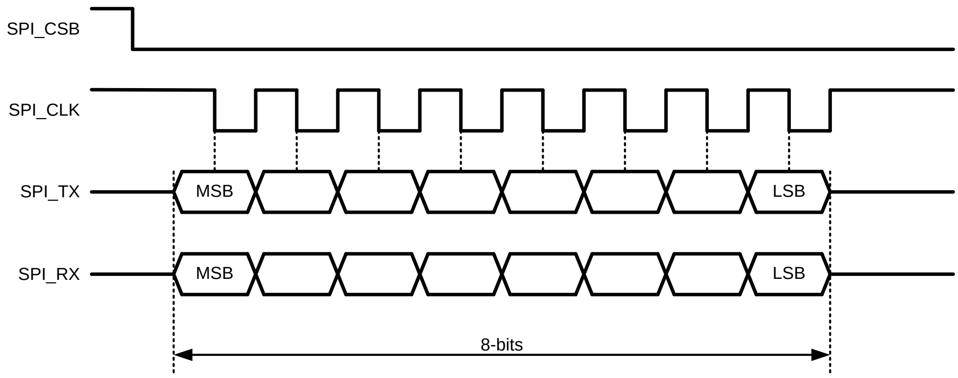


Figure 5-47 Master Mode, POLARITY=1, PHASE=0

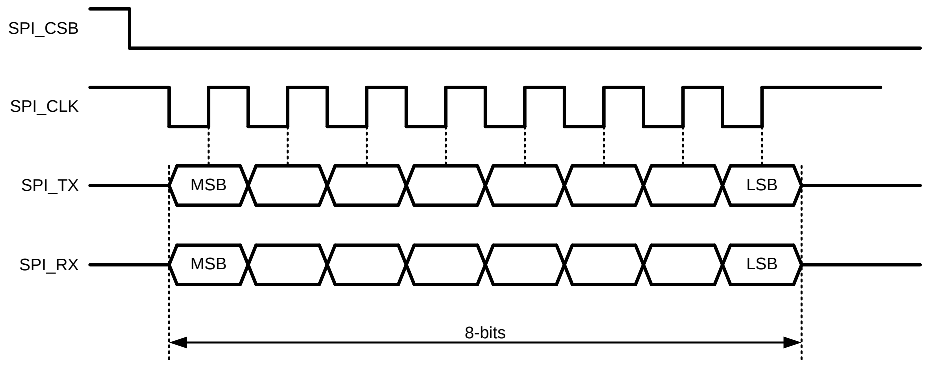


Figure 5-48 Master Mode, POLARITY=1, PHASE=1

5.11.1. SPI Releated Register

SPI_CTRL			Page: 0 / Address: 0x9A		SPI Control Register			
Bit	7	6	5	4	3	2	1	0
Function	POLARITY	PHASE	CSB_KEEP	SPI_CLK_SEL[1:0]		SPI_EN	SPI_MODE	SPI_START
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7	POLARITY	R/W	SPI CLK initial state 0: low state 1: high state	
6	PHASE	R/W	SPI CLK type control 0: 1st edge sample 1: 2nd edge sample	
5	CSB_KEEP	R/W	SPI CSB keep low control	
4:3	SPI_CLK_SEL[1:0]	R/W	SPI Clock output selection: 00: system clock / 2 01: system clock / 4 10: system clock / 8 11: system clock / 16	
2	SPI_EN	R/W	SPI IO state enable When SPI_STS.IOSW = 0 , SPI signals forward to P2[6]: SPI_CLK P2[7]: SPI_CSB P3[0]: SPI_RX P3[1]: SPI_TX When SPI_STS.IOSW = 1 , SPI signals forward to P3[5]: SPI_CLK P3[6]: SPI_CSB P3[7]: SPI_RX P4[0]: SPI_TX	
1	SPI_MODE	R/W	SPI operation mode. 0: Master 1:Slaver	
0	SPI_START	R/W	SPI enable(W)/SPI busy flag(R)	

Table 5-175 SPI register

SPI_STS			Page: 0 / Address: 0x9B		SPI Status Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_INTEN	--	--	--	--	--	RX_DONE	TX_DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SPI_INTEN	R/W	SPI interrupt enable 0: disabled 1: enabled	
6:2	-	R/W	Reserved	

Bit	Function	Type	Description	Condition
1	RX_DONE	R/W	SPI finished data receiving with slaver mode. read: 0: Idle / Busy 1:Done write: 0: clears this bit 1: no effect	
0	TX_DONE	R/W	SPI finished data transmission with master mode. 0: Idle / Busy 1:Done write: 0: clears this bit 1: no effect	

Table 5-176 SPI_STS register

SPI_TXD			Page: 0 / Address: 0x9C		SPI Transmission Data Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_TXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPI_TXD[7:0]	R/W	SPI transmission data	

Table 5-177 SPI_TXD register

SPI_RXD			Page: 0 / Address: 0x9D		SPI Receive Data Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_RXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPI_RXD	R/W	SPI receive data	

Table 5-178 SPI_RXD register

5.12. ADC

There is one Analog-to-Digital-Converter (ADC) embedded in GPM8F3331B. It provides general purpose usages such as any other analog functions.

- 13 channels, 12-bit resolution (11-bit no-missing code) ADC
- Supports programming sample hold and ADC clock function
- Supports internal VSS channel for data correction
- Supports Offset calibrate
- DMA request generation during regular channel conversion
- Supports one channel window trigger function

5.12.1. ADC Controller

Total of 13 channels of 12-bit SAR ADC per set are built in GPM8F3331B. These thirteen channels are very suitable for system voltage detection and other general-purpose usages. Figure 5-49 shows the ADC control block. The ADC_CLK that divided by a pre-scaler and it must not exceed 18 MHz. The ADC_CLK is synchronous with the system clock. The one ADC conversion time include 3 parts, ADC sample hold (SH) time, conversion time (ADC clock 13T) and REG_SEQ_GAP, the detail waveform see the Figure 5-50.

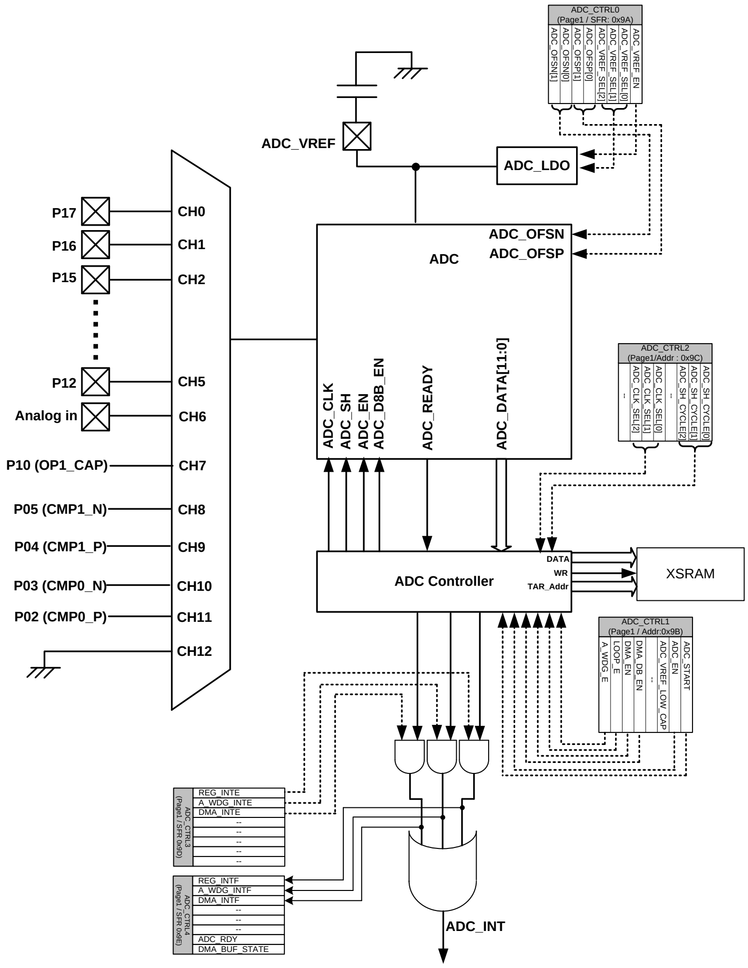


Figure 5-49 ADC Control block

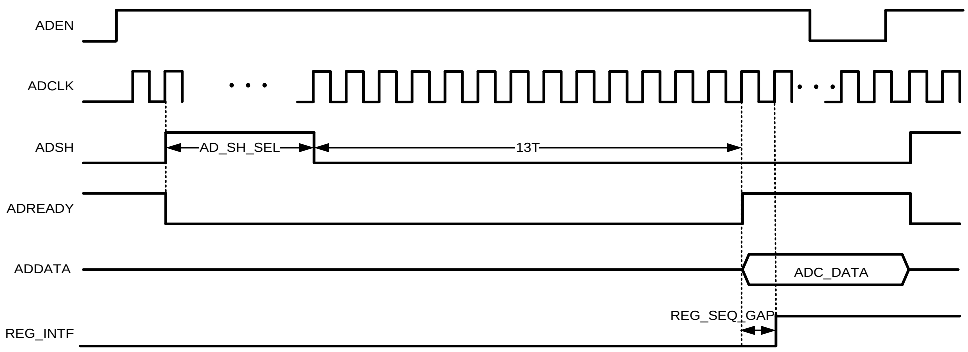


Figure 5-50 ADC conversion waveform

5.12.1.1. Channel Selection

In the GPM8F3331B has up to 13 multiplexed channels. The regular mode is composed of up to 13 conversions. The regular channels and their order in the conversion sequence must be selection in ADC_REG_SEQ0~6 registers. The total number of conversions in regular mode must be written in the ADC_CTRL5.REG_CH_NUM. Table 5-179 is the ADC Channel mapping.

Channel	ADC Channel Mapping
0	P17
1	P16
2	P15
3	P14
4	P13
5	P12
6	Analog input
7	P10
8	P05 (CMP1_N)
9	P04(CMP1_P)
10	P03(CMP0_N)
11	P02(CMP0_P)
12	VSS

Table 5-179 ADC Channel mapping

5.12.1.2. Regular mode with loop function disable

In regular conversion mode with loop function disable, the ADC does one conversion. This mode is started by setting ADC_CTRL1.ADC_START only. The conversion of the selected channel is completed.

• If a regular channel was converted:

1. The converted data is stored in the 16-bit ADC _REG_DATA register.
2. The ADC_CTRL4.REG_INTF flag is set.
3. An interrupt is generated if the ADC_CTRL3.REG_INTE is set.
4. User clear ADC_CTRL4.REG_INTF flag by write ADC_CTRL0.REG_INTF to 0.

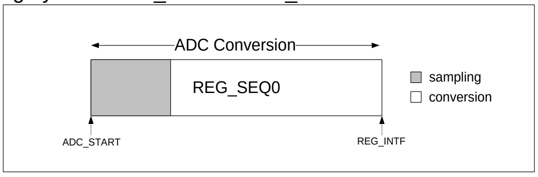


Figure 5-51 one regular mode with loop function disable

• If N regular channel were converted:

1. The converted data is stored in the 16-bit ADC_REG_DATA register
2. The ADC_CTRL4.REG_INTF flag is set
3. An interrupt is generated if the ADC3_CTRL0.REG_INTE is set.
4. User clear ADC_CTRL4.REG_INTF flag by write ADC_CTRL4.REG_INTF to 0.
5. Past some ADC_CLK cycles that was set in ADC_CTRL5.REG_SEQ_GAP, do next conversion until all of the regular channel are finished.

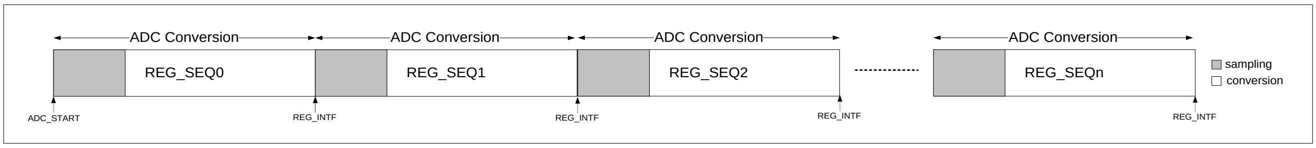


Figure 5-52 N-regular mode conversion with loop function disable

5.12.1.3. Regular mode with loop function enable

In regular conversion mode with loop function enable, the ADC will repeat the channel conversion action. This mode is started by setting the ADC_CTRL1.ADC_START. Before start ADC conversion, user must set ADC_CTRL1.LOOP_E to 1. The data conversion will be triggered by hardware automatically until software disable ADC or set ADC_CTRL1.LOOP_E to 0.

• If only one regular channel was selected:

1. The converted data is stored in the 16-bit ADC_REG_DATA register.
2. The ADC_CTRL4.REG_INTF flag is set.
3. An interrupt is generated if the ADC_CTRL3.REG_INTE is set.
4. User clear ADC_CTRL4.REG_INTF flag by write ADC_CTRL4.REG_INTF to 0.
5. Past some ADC_CLK cycles that were set in ADC_CTRL5.REG_SEQ_GAP, does next iteration until software disable ADC or set ADC _CTRL1.LOOP_E to 0.

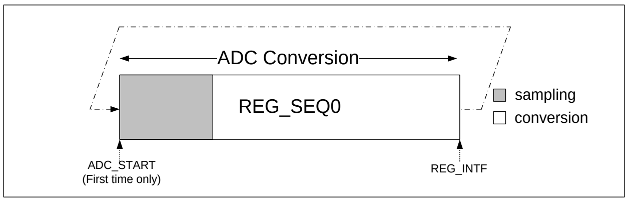


Figure 5-53 one regular mode with loop function enable

• If N regular channel were converted:

1. The converted data is stored in the 16-bit ADC_REG_DATA register
2. The ADC_CTRL4.REG_INTF flag is set.
3. An interrupt is generated if the ADC_CTRL3.REG_INTE is set.
4. User clear ADC_CTRL4.REG_INTF flag by write ADC_CTRL4.REG_INTF to 0.
5. Past some ADC_CLK cycles that were set in ADC_CTRL5.REG_SEQ_GAP, do next conversion until all of the regular channel are finished.
6. Past some ADC_CLK cycles that were set in ADC_CTRL5.REG_SEQ_GAP, does next iteration until software disable ADC or set ADC _CTRL1.LOOP_E to 0.

5.12.1.4. Regular mode with DMA

In regular mode, since converted data are stored in ADC_REG_DATA. User can read data by CPU access. In addition , DMA access is another path. The DMA access works for multiple regular channels. This prevents the data that stored in ADC_REG_DATA being overwritten.

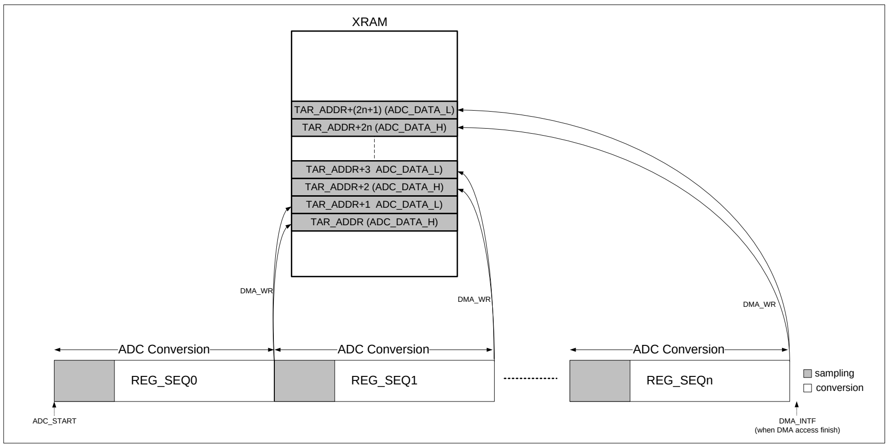


Figure 5-54 Regular mode with DMA

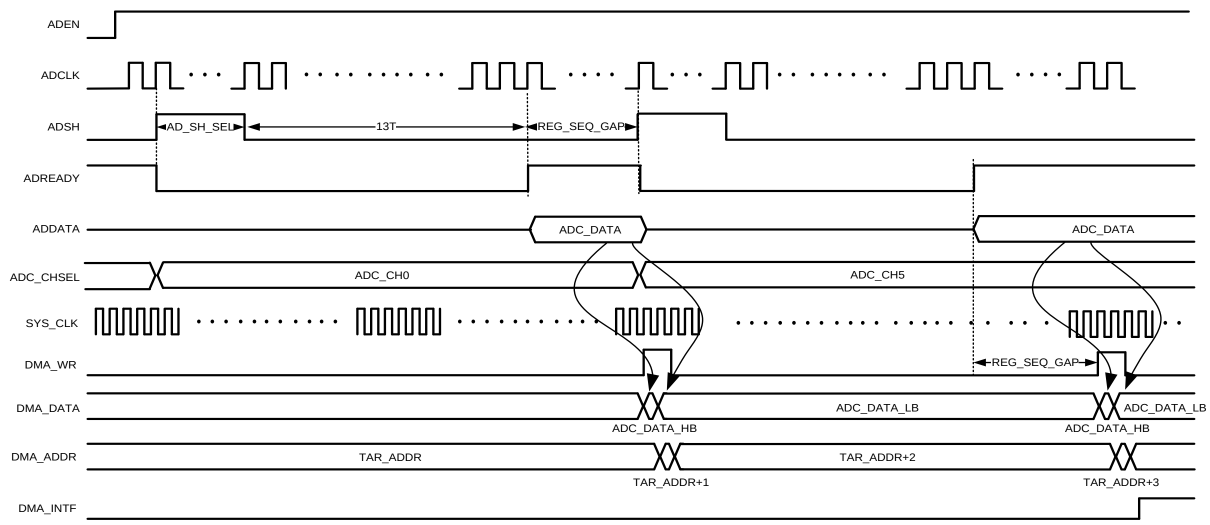


Figure 5-55 The timing diagram of ADC DMA function

GMP8F3331B supports DMA double buffer function, when user set the ADC_CTRL1.DMA_DB_EN to 1. When ADC_CTRL4.DMA_BUF_STATE indicates 0, if user starts or restarts ADC with DMA function, the data access will auto reload target address to storage. If ADC_CTRL4.DMA_BUF_STATE indicates 1 and user restarts the ADC with DMA functio, the data access will continue the last end address storage. The **Figure 5-56** is the DMA double buffer application detail waveform.

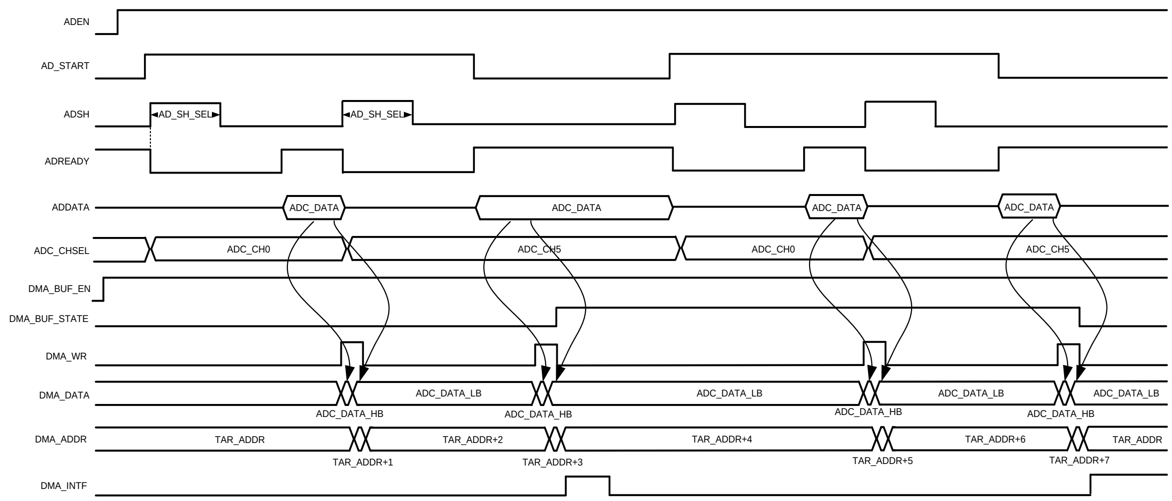


Figure 5-56 The timing diagram of ADC DMA double buffer function

5.12.1.5. Analog watchdog function

ADC provides a set of channel mechanism to measure voltage range of input signal. The ADC_CTRL4.A_WDG_INTF are set if the analog voltage converted by the ADC is below ADC_WDG_TH.LB or above ADC_WDG_TH.HB. The interrupts can be enabled by using the ADCx_CTRL3.A_WDG_INTE and A_WDG_CHSEL equal ADC conversion channel. In addition, the threshold setting is independent of the ADC_WDG_TH setting. The comparison is done before the data alignment and after offset calibration.

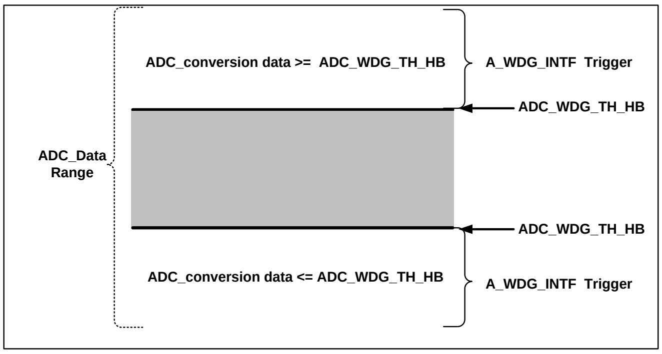


Figure 5-57 ADC watchdog function

5.12.1.6. Data Alignment

ADC provides two data alignment types, left-aligned or right-aligned. The ADC_CTRL6.DATALIGN bit selects the alignment of data stored after conversion and offset calibration. The following figures show some examples of the different data alignments.

ADC_REG_DATA_H								ADC_REG_DATA_L							
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

Figure 5-58 Left-aligned (ADC_CTRL6.DATALIGN = 0)

ADC_REG_DATA_H								ADC_REG_DATA_L							
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 5-59 Right-aligned (ADC_CTRL6.DATALIGN = 1)

5.12.1.7. Offset Calibration

ADC provides offset calibration function. The user can cancel the ADC offset data by setting ADC_OFSET_VAL. Before that, user needs to switch the ADC to VSS channel to obtain reference data. And fill the data into ADC_OFSET_VAL, then set ADC_CTRL6.ADC_OFSET_CAL_EN to complete offset calibration of ADC.

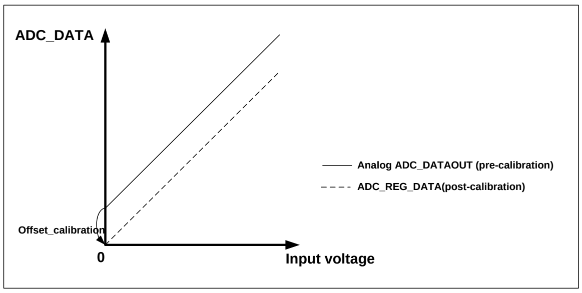


Figure 5-60 Offset calibration

5.12.2. ADC Related Register

ADC_CTRL0			**Page:1 / Address: 0x9A**		**ADC Control Register 0**			
Bit	7	6	5	4	3	2	1	0
Function	ADC_OFSN		ADC_OFSP		ADC_VREF_SEL			ADC_ VREFE
Default	0	0	0	0	0	0	0	0
Key Code								

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>ADC_OFSN</td><td>R/W</td><td>ADC offset negative adjustment
<table>
<tr><td>ADC_OFSN</td><td>Adjustment Range</td></tr>
<tr><td>00</td><td>A (default value)</td></tr>
<tr><td>01</td><td>A - B</td></tr>
<tr><td>10</td><td>A - 2B</td></tr>
<tr><td>11</td><td>A - 3B</td></tr>
</table>
Note: The value A and B is dependent on actual situation.</td><td></td></tr>
<tr><td>5:0</td><td>ADC_OFSP</td><td>R/W</td><td>ADC offset positive adjustment
<table>
<tr><td>ADC_OFSP</td><td>Adjustment Range</td></tr>
<tr><td>00</td><td>C (default value)</td></tr>
<tr><td>01</td><td>C + D</td></tr>
<tr><td>10</td><td>C + 2D</td></tr>
<tr><td>11</td><td>C + 3D</td></tr>
</table>
Note: The value C and D is dependent on actual situation.</td><td></td></tr>
<tr><td>3:1</td><td>ADC_VREF_SEL</td><td>R/W</td><td>ADC reference voltage select
<table>
<tr><td>ADC_VREF_SEL</td><td>ADC_VREF_output voltage</td></tr>
<tr><td>000</td><td>1.8V</td></tr>
<tr><td>001</td><td>2.0V</td></tr>
<tr><td>010</td><td>3.0V</td></tr>
<tr><td>011</td><td>3.3V</td></tr>
<tr><td>100</td><td>4.0V</td></tr>
<tr><td>101</td><td>4.2V</td></tr>
<tr><td>110</td><td>4.6V</td></tr>
<tr><td>111</td><td>VDD</td></tr>
</table></td><td></td></tr>
<tr><td>0</td><td>ADC_VREF_EN</td><td>R/W</td><td>ADC reference voltage enable
0: Disabled
1: Enabled
Note: The reference voltage of ADC should be injected via ADC_VREF PAD if ADC_VREF_E is disabled.</td><td></td></tr>
</table>

Table 5-180 ADC_CTRL0 register

ADC_CTRL1			**Page:1 / Address: 0x9B**		**ADC Control Register 1**			
Bit	7	6	5	4	3	2	1	0
Function	A_WDG_ _EN	LOOP_ EN	DMA_EN	DMA_DB _EN	--	ADC_VREF_ Low_CAP	ADC_EN	ADC_ START
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7	A_WDGR_EN	R/W	Analog Watchdog enable on regular channel 0: Disabled 1: Enabled	
6	LOOP_EN	R/W	ADC loop scan enable bit 0: Single conversion mode 1: Loop scan conversion mode Note: This bit is available in regular mode only	
5	DMA_EN	R/W	DMA request enable 0: DMA mode disabled 1: DMA mode enabled	
4	DMA_DB _EN	R/W	DMA Double Buffer Enable 0: Disabled 1: Enable	
3	--	R/W	Reserved	
2	ADC_VREF_ Low_CAP	R/w	ADC_VREF_Cap select 0: External Cap Range is 1uF~4.7uF 1: External Cap Range is 0.1uF~1uF	
1	ADC_EN	R/W	ADC analog block enable 0: Disabled 1: Enabled Note: User should set this bit enable before running ADC function.	
0	ADC_START	R/W	Software start bit 0: Disabled 1: Enabled (start conversion of regular channel) Note: This bit is available in regular mode only. This bit will be cleared by hardware, when LOOP_E is set to 0 and all of regular scan were be finished. If LOOP_E is set to 1, then signal be cleared by software.	

Table 5-181 ADC_CTRL1 register

ADC_CTRL2			**Page:1 / Address: 0x9C**		**ADC Control Register 2**			
Bit	7	6	5	4	3	2	1	0
Function	--	ADC_CLK_SEL			--	ADC_SH_SEL		
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:4	ADC_CLK_SEL	R/W	ADC clock select bits ADC_CLK_SEL[2:0] → System clock divide by: 000: 2 001: 3 010: 4 011: 5 100: 6 101: 7 110: 12 111: 16	

Bit	Function	Type	Description	Condition
3	--	R/W	Reserved	
2:0	ADC_SH_SEL	R/W	ADC sample and hold cycle select ADC_SH_SEL[2:0] / Cycles of ADC clock: 000: 1 001: 2 010: 3 011: 4 100: 10 101: 50 110: 100 111: 200	

Table 5-182 ADC_CTRL2 register

ADC_CTRL3			Page:1 / Address: 0x9D		ADC Control Register 3			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	DMA_INTE	A_WDG_INTE	REG_INTE
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2	DMA_INTE	R/W	DMA Finish interrupt enable 0: Disabled 1: Enabled	
1	A_WDG_INTE	R/W	Analog Watchdog interrupt enable on regular channel 0: Disabled 1: Enabled	
0	REG_INTE	R/W	Regular mode interrupt enable 0: Disabled 1: Enabled	

Table 5-183 ADC_CTRL3 register

ADC_CTRL4			Page:1 / Address: 0x9E		ADC Control Register 4			
Bit	7	6	5	4	3	2	1	0
Function	DMA_BUF_STATE	ADC_RDY	--	--	--	DMA_INTF	A_WDG_INTF	REG_INTF
Default	0	1	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7	DMA_BUF_STATE	R	DMA_BUFFER State 0: DMA write A buffer state or idle state 1: DMA write B buffer state	
6	ADC_RDY	R	ADC finish signal	

Bit	Function	Type	Description	Condition
			0: ADC is idle or sample and hold or conversion 1: ADC data conversion done	
5:3	--	R/W	Reserved	
2	DMA_INTF	R/W	DMA finish interrupt flag Read : 0: No analog watch dog occurred 1: Analog watch dog occurred Write : 0: Clear this flag 1: No effect	
1	A_WDG_INTF	R/W	Analog watchdog interrupt flag on regular channel Read : 0: No analog watchdog occurred 1: Analog watchdog occurred Write : 0: Clear this flag 1: No effect	
0	REG_INTF	R/W	Regular conversion interrupt flag Read : 0: No regular conversion was finished 1: Regular conversion has finished Write : 0: Clear this flag 1: No effect	

Table 5-184 ADC_CTRL4 register

ADC_CTRL5			**Page:1 / Address: 0x9F**		**ADC Control Register 5**			
Bit	7	6	5	4	3	2	1	0
Function	REG_SEQ_GAP			REG_CH_NUM				REG_E
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:5	REG_SEQ_GAP	R/W	Regular sequence gap select bits REG_SEQ_GAP[2:0] → Cycles of ADCx clock 000 → 0 001 → 1 010 → 2 011 → 3 100 → 4 101 → 5 110 → 6 111 → 7 Note:	

Bit	Function	Type	Description	Condition
4:1	REG_CH_NUM	R/W	Channel number during regular sequence Note: The physical channel number is ADCx_CTRL1.REG_CH_NUM + 1. In addition, the scan sequence is always being started from sequence-0.	
0	REG_E	R/W	Regular mode enable bit 0: Disabled 1: Enabled Note: Before use regular sequence, user must set ADC _CTRL5.REG_E to 1 first. Then set ADC _CTRL.SFT1_ADC_START to 1 to start regular sequence.	

Table 5-185 ADC_CTRL5 register

ADC_CTRL6			**Page:1 / Address: 0xA2**		**ADC Control Register 6**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	OFSET_CAL_TYP	ADC_OFSET_CAL_EN	ADC_D8B_EN	DATA_ALIGN
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	OFSET_CAL_TYP	R/W	Offset calibration type 0: ADC_data – offset_cal data 1: ADC_ data + offset cal data	
2	ADC_OFSET_CAL_EN	R/W	ADC offset calibration enable bit 0: Disable 1: Enable	
1	ADC_D8B_EN	R/W	ADC 8-bit data mode enable bit 0: Disabled 2. 1: Enabled	
0	DATA_ALIGN	R/W	ADC output data alignment 0: Left alignment 1: Right alignment	

Table 5-186 ADC_CTRL6 register

ADC_REG_DATA_L			**Page:1 / Address: 0xA3**		**ADC REG DATA Low Byte**			
Bit	7	6	5	4	3	2	1	0
Function	ADC_REG_DATA_L							
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:0	ADC_REG_DATA_L	R	ADC regular data low byte	

Table 5-187 ADC_REG_DATA_L register

ADC_REG_DATA_H			Page:1 / Address: 0xA4		ADC REG_DATA High Byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC REG_DATA High Byte							
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:0	ADC_REG_DATA_H	R	ADC regular data high byte	

Table 5-188 ADC_REG_DATA_H register

ADC_REG_SEQ0			Page:1 / Address: 0xA5		ADC Regular Sequence Register0			
Bit	7	6	5	4	3	2	1	0
Function	REG_SEQ1				REG_SEQ0			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	REG_SEQ1	R/W	The 1st conversion in regular sequence This indicates which channel in 1st regular sequence	
3:0	REG_SEQ0	R/W	The 0th conversion in regular sequence This indicates which channel in 0th regular sequence	

Table 5-189 ADC_REG_SEQ0 register

ADC_REG_SEQ1			Page:1 / Address: 0xA6		ADC Regular Sequence Register1			
Bit	7	6	5	4	3	2	1	0
Function	REG_SEQ3				REG_SEQ2			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	REG_SEQ3	R/W	The 3st conversion in regular sequence This indicates which channel in 3st regular sequence	
3:0	REG_SEQ2	R/W	The 2th conversion in regular sequence This indicates which channel in 2th regular sequence	

Table 5-190 ADC_REG_SEQ1 register

ADC_REG_SEQ2			Page:1 / Address: 0xA7		ADC Regular Sequence Register2			
Bit	7	6	5	4	3	2	1	0
Function	REG_SEQ5				REG_SEQ4			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	REG_SEQ5	R/W	The 5st conversion in regular sequence This indicates which channel in 5st regular sequence	

Bit	Function	Type	Description	Condition
3:0	REG_SEQ4	R/W	The 4th conversion in regular sequence This indicates which channel in 4th regular sequence	

Table 5-191 ADC_REG_SEQ2 register

ADC_REG_SEQ3				**Page:1 / Address: 0xAA**		**ADC Regular Sequence Register3**		
Bit	7	6	5	4	3	2	1	0
Function	REG_SEQ7				REG_SEQ6			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	REG_SEQ7	R/W	The 7st conversion in regular sequence This indicates which channel in 7st regular sequence	
3:0	REG_SEQ6	R/W	The 6th conversion in regular sequence This indicates which channel in 6th regular sequence	

Table 5-192 ADC_REG_SEQ3 register

ADC_REG_SEQ4				**Page:1 / Address: 0xAB**		**ADC Regular Sequence Register4**		
Bit	7	6	5	4	3	2	1	0
Function	REG_SEQ9				REG_SEQ8			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	REG_SEQ9	R/W	The 9st conversion in regular sequence This indicates which channel in 9st regular sequence	
3:0	REG_SEQ8	R/W	The 8th conversion in regular sequence This indicates which channel in 8th regular sequence	

Table 5-193 ADC_REG_SEQ4 register

ADC_REG_SEQ5				**Page:1 / Address: 0xAC**		**ADC Regular Sequence Register5**		
Bit	7	6	5	4	3	2	1	0
Function	REG_SEQ11				REG_SEQ10			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	REG_SEQ11	R/W	The 11st conversion in regular sequence This indicates which channel in 11st regular sequence	
3:0	REG_SEQ10	R/W	The 10th conversion in regular sequence This indicates which channel in 10th regular sequence	

Table 5-194 ADC_REG_SEQ5 register

ADC_REG_SEQ6			Page:1 / Address: 0xAD		ADC Regular Sequence Register6			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	REG_SEQ12			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	REG_SEQ12	R/W	The 12th conversion in regular sequence This indicates which channel in 12th regular sequence	

Table 5-195 ADC_REG_SEQ6 register

ADC_WDG_TH_HB_L			Page:1 / Address: 0xB2		ADC Watchdog Threshold High Boundary- Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC_WDG_TH_HB_L							
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:0	ADC_WDG_TH_HB_L	R/W	Analog watchdog threshold high boundary low byte	

Table 5-196 ADC_WDG_TH_HB_L register

ADC_WDG_TH_HB_H			Page:1 / Address: 0xB3		ADC Watchdog Threshold High Boundary - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	ADC_WDG_TH_HB_H			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	ADC_WDG_TH_HB_H	R/W	Analog watchdog threshold high boundary high byte	

Table 5-197 ADC_WDG_TH_HB_H register

ADC_WDG_TH_LB_L			Page:1 / Address: 0xB4		ADC Watchdog Threshold Low Boundary - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC_WDG_TH_LB_L							
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:0	ADC_WDG_TH_LB_L	R/W	Analog watchdog threshold low boundary low byte	

Table 5-198 ADC_WDG_TH_LB_L register

ADC_WDG_TH_LB_H			Page:1 / Address: 0xB5		ADC Watchdog Threshold Low Boundary - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	ADC_WDG_TH_LB_H			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	ADC_WDG_TH_LB_H	R/W	Analog watchdog threshold low boundary high byte	

Table 5-199 ADC_WDG_TH_LB_H register

ADC_WDG_CHSEL			Page:1 / Address: 0xB6		ADC Watchdog Channel Select			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	ADC_WDG_CHSEL			
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	ADC_WDG_CHSEL	R/W	Analog watchdog channel select	

Table 5-200 ADC_WDG_CHSEL register

ADC_DMA_TAR_ADDR_L			Page:1 / Address: 0xBA		ADC DMA Target Address_L			
Bit	7	6	5	4	3	2	1	0
Function	DMA_TAR_ADDR_L							
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:0	DMA_TAR_ADDR_L	R/W	ADC DMA target address low byte	

Table 5-201 ADC_DMA_TAR_ADDR_L register

ADC_DMA_TAR_ADDR_H			Page:1 / Address: 0xBB		ADC DMA Target Address_H			
Bit	7	6	5	4	3	2	1	0
Function	DMA_TAR_ADDR_H							
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:0	DMA_TAR_ADDR_H	R/W	ADC DMA target address high byte	

Table 5-202 ADC_DMA_TAR_ADDR_H register

ADC_OFSET_VAL			Page:1 / Address: 0xBC		ADC Offset Value - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC_OFSET_VAL							
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:0	ADC_OFSET_VAL	R/W	ADC offset value (offset calibration range 0~255)	

Table 5-203 ADC_OFSET_VAL register

5.13. I2C Unit

The GPM8F3331B incorporates an Inter integrated circuit (I2C) interfaces. The I2C is used for attaching lower-speed peripheral ICs to processors and microcontroller in short-distance. The I2C uses only two bidirectional open-drain lines, that are serial data line (SDA) and serial clock line (SCL). Logic 0 is output by sinking the bus to ground, and logic 1 is output by letting the bus to floating state, and via the pull-up resistor pulls it to high.

5.13.1. Feature

- ❑ Multi-master capability
- ❑ Supports I2C master and slave mode
- ❑ Generation and detection of 7-bit/10-bit addressing and General Call
- ❑ Optional clock

5.13.2. Block Diagram

The Figure 5-61 is the block diagram of I2C.

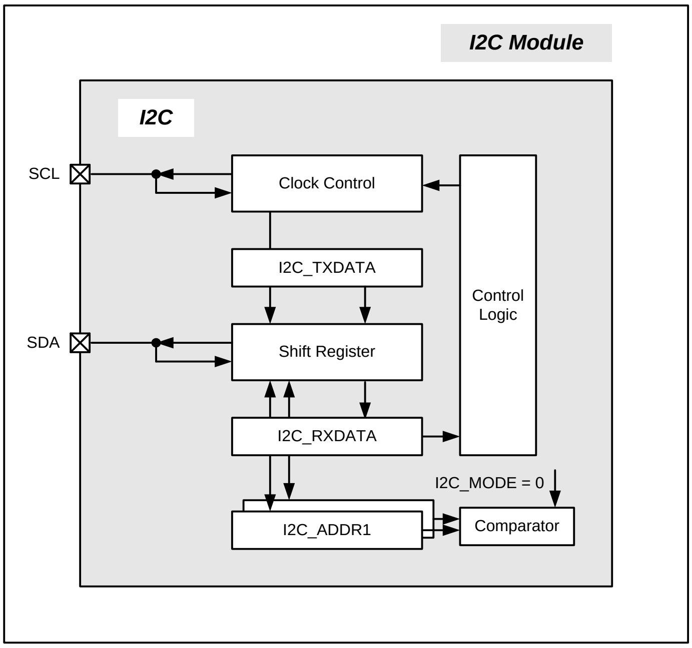


Figure 5-61 I2C block diagram

5.13.3. Function Description

In GPM8F3331B, I2C supports 7-bit or 10-bit (depending on the device used) address space. Only two wires (SCK and SDA) are needed to implement the protocol. In multi-master I2C-bus mode, multiple microprocessors can receive or transmit serial data to or from slave devices. If more than one master tries to control the line simultaneously, an arbitration mechanism is used to judge which one is bus owner. In I2C controller, four transfer modes are supported:

- ❑ master transmit – master is sending data to a slave
- ❑ master receive – master is receiving data from a slave
- ❑ slave transmit – slave is sending data to the master
- ❑ slave receive – slave is receiving data from the master

Formats of I2C frame

Figure 5-62 shows the frame format of I2C.

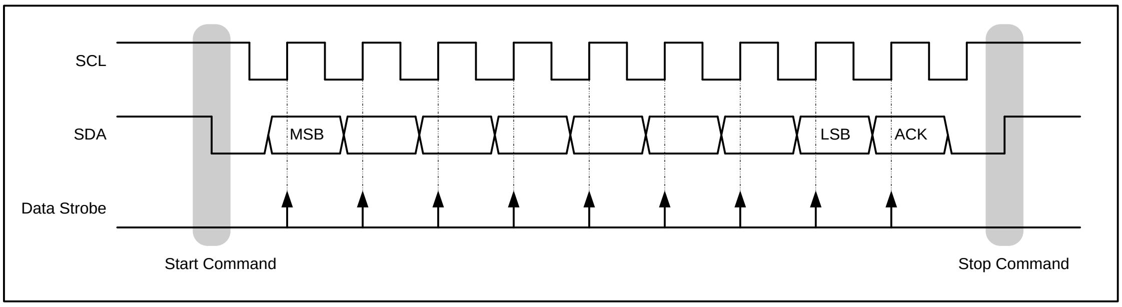


Figure 5-62 The frame format of I2C

5.13.4 Master Mode

5.13.4.1 Arbitration lost

A master may start a transfer only if the bus is free. Arbitration takes place on the SDA line, while the SCL line is at the HIGH level. In such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level. The **I2C_STS0.ARB_LOST** is set by hardware when the I2C interface detects an arbitration lost. Then, I2C controller switches from master to slave mode automatically. A master that still generate clock pulses until the end of the packet when it loses the arbitration. Figure shows an arbitration mechanism of two masters.

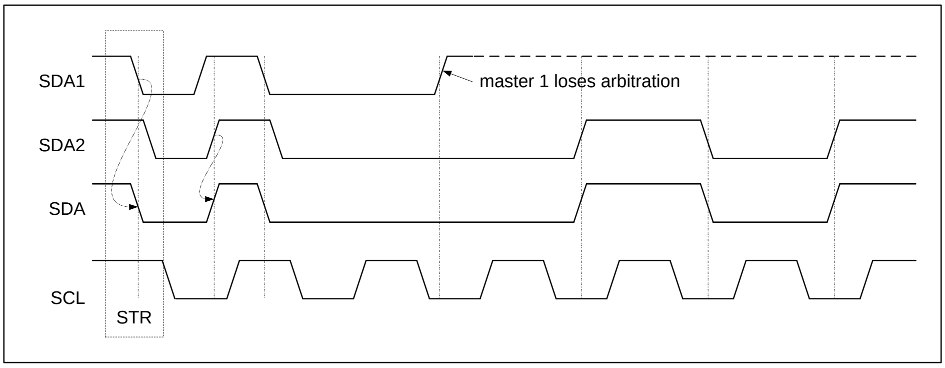


Figure 5-63 The arbitration mechanism of two masters.

5.13.4.2 I2C master transmitter

In master transmitter, before using I2C transmits function, user must fill in transfer data, slave address and set **I2C_CTRL0.I2C_EN** to 1. In addition, master can inform slave this transfer is a write transfer by set **I2C_ADDR1.R_W** to 0. Then, I2C sends out data immediately when **I2C_CTRL0.I2C_TRG** is set to 1. During an I2C transmission, data shifts out most significant bit first on the SDA pin. **I2C_STS0.TRS_DONE** flag will be set to 1 when data and acknowledge bit transfer are finished. Before next transmission, user must clear this bit by software. And, trigger next transfer by fill in latest data into **I2C_TXDATA**. If user wants to terminate I2C transmission, set **I2C_CTRL0.MST_STP** and **I2C_CTRL0.I2C_TRG** to 1 that will execute a stop command transfer. Below figures show the transfer bus diagram and transfer sequence flowchart for master transmitter.

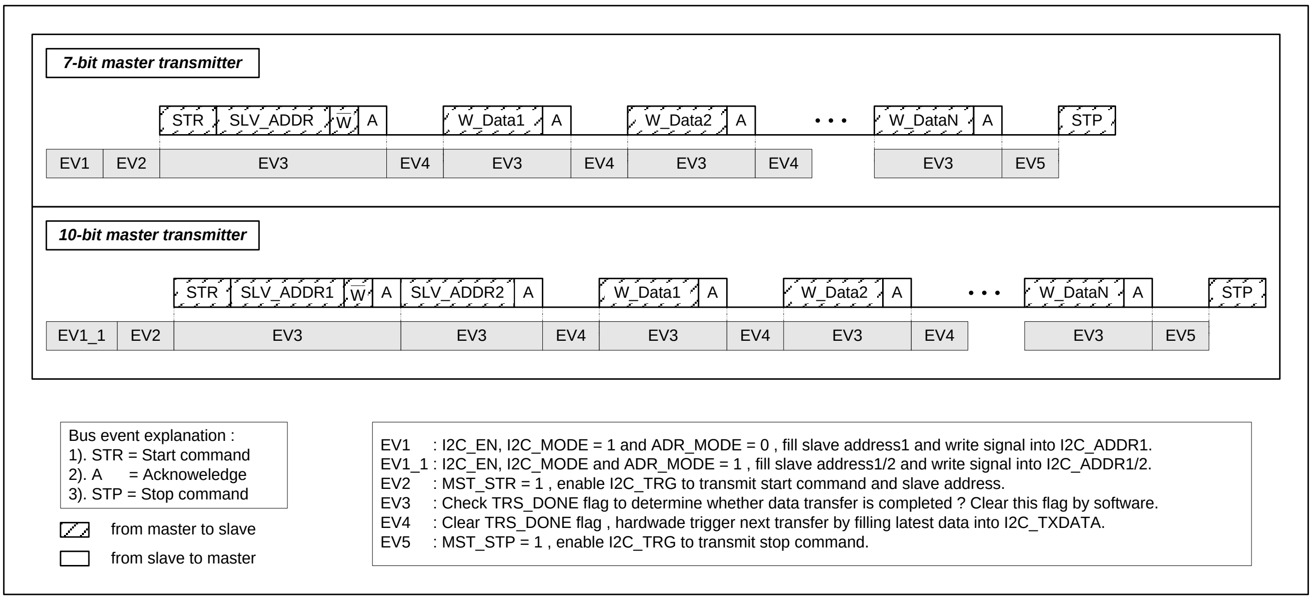


Figure 5-64 I2C transfer bus diagram for master transmitter

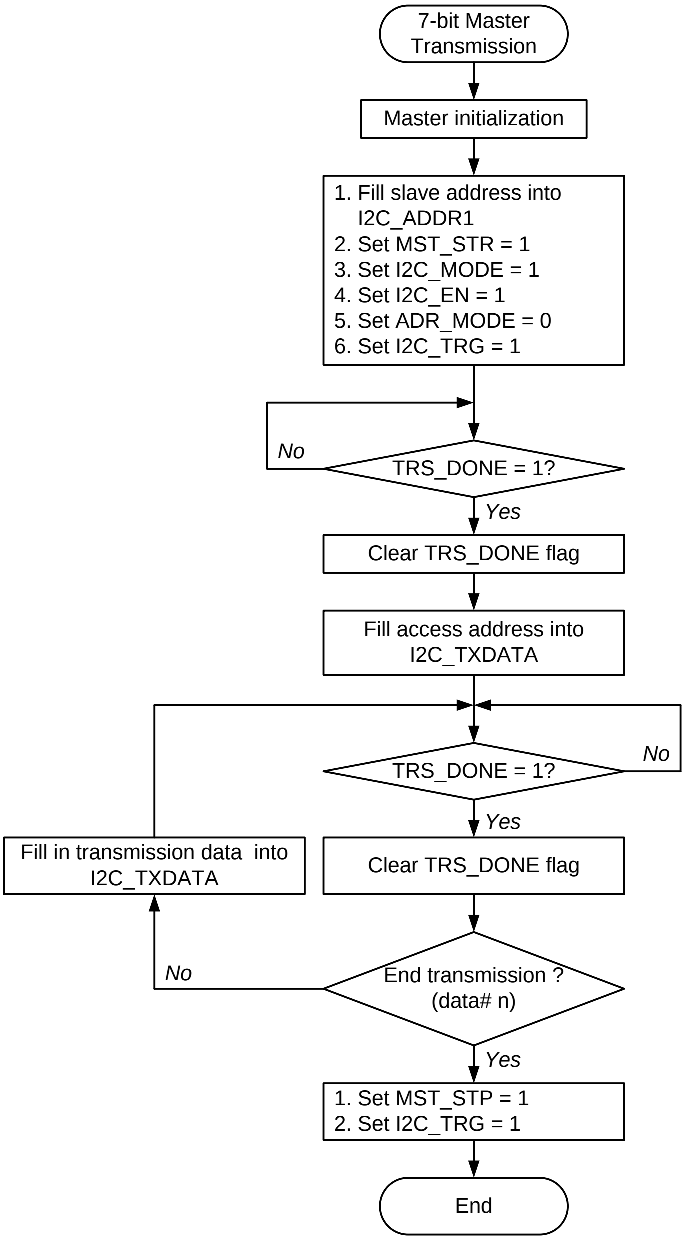


Figure 5-65 I2C transfer sequence flowchart for master transmitter (7-bit mode)

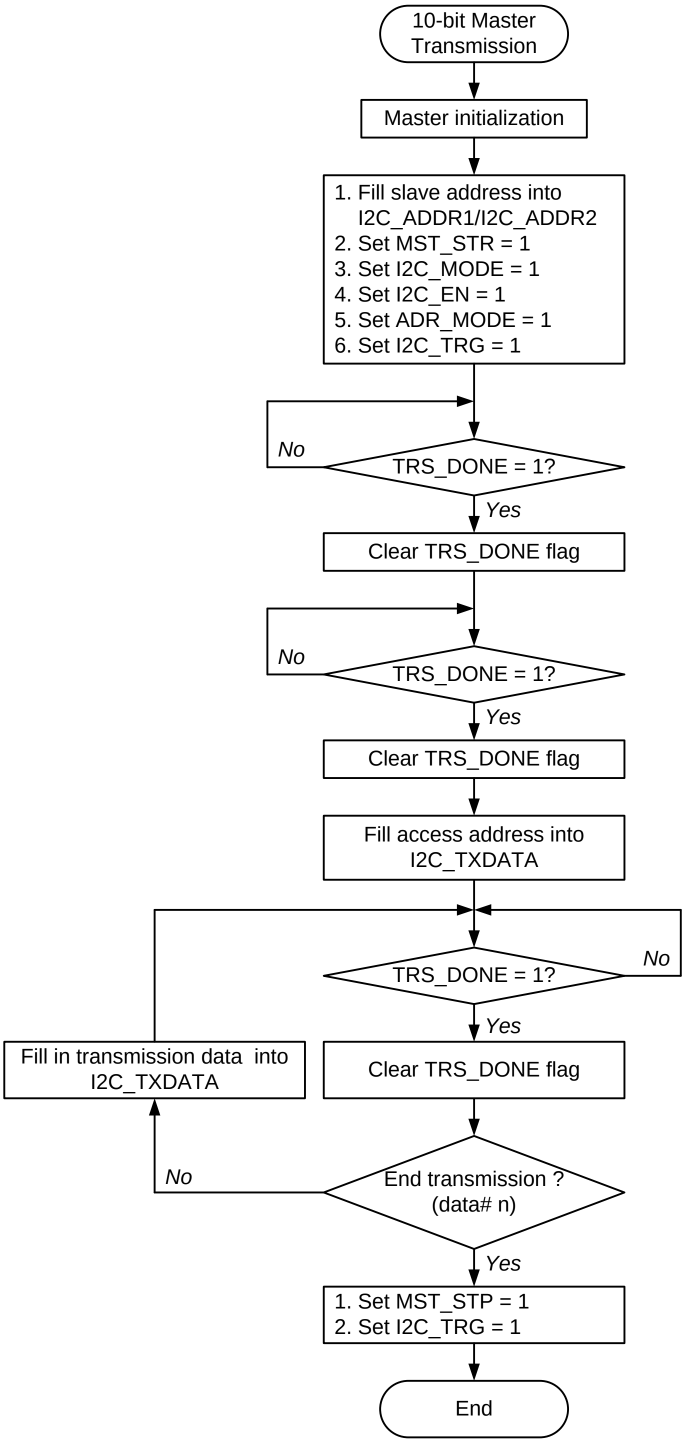


Figure 5-66 I2C transfer sequence flowchart for master transmitter (10-bit mode)

5.13.4.3 I2C master receiver

In master receiver, before using I2C receives function, user must fill slave address in **I2C_ADDR1/2** and set **I2C_CTRL0.I2C_EN** to 1. In addition, master informs slave this is a write transfer by set **I2C_ADDR1.R_W** to 0. Once master received acknowledge, it indicates slave is ready to receive transfer data. Master will execute read transfer by sending a re-start command with slave address. Once master ready to receive data, set **I2C_TRG** to 1 will start data receiving. During an I2C transmission, data shifts in most significant bit first from the SDA pin. The **I2C_STS0.TRS_DONE** will be set to 1 when data and acknowledge bit transfer are finished. Before next transmission, user must clear this bit by software. And, trigger next transfer by read data from **I2C_RXDATA**. If user wants to terminate I2C reception, set **I2C_CTRL0.MST_NACK** to 1 before final read transfer. After final transfer done, controller send a stop command by set **I2C_CTRL0.MST_STP** and **I2C_CTRL0.I2C_TRG** to 1. Below figures show the transfer bus diagram and transfer sequence flowchart for master receiver.

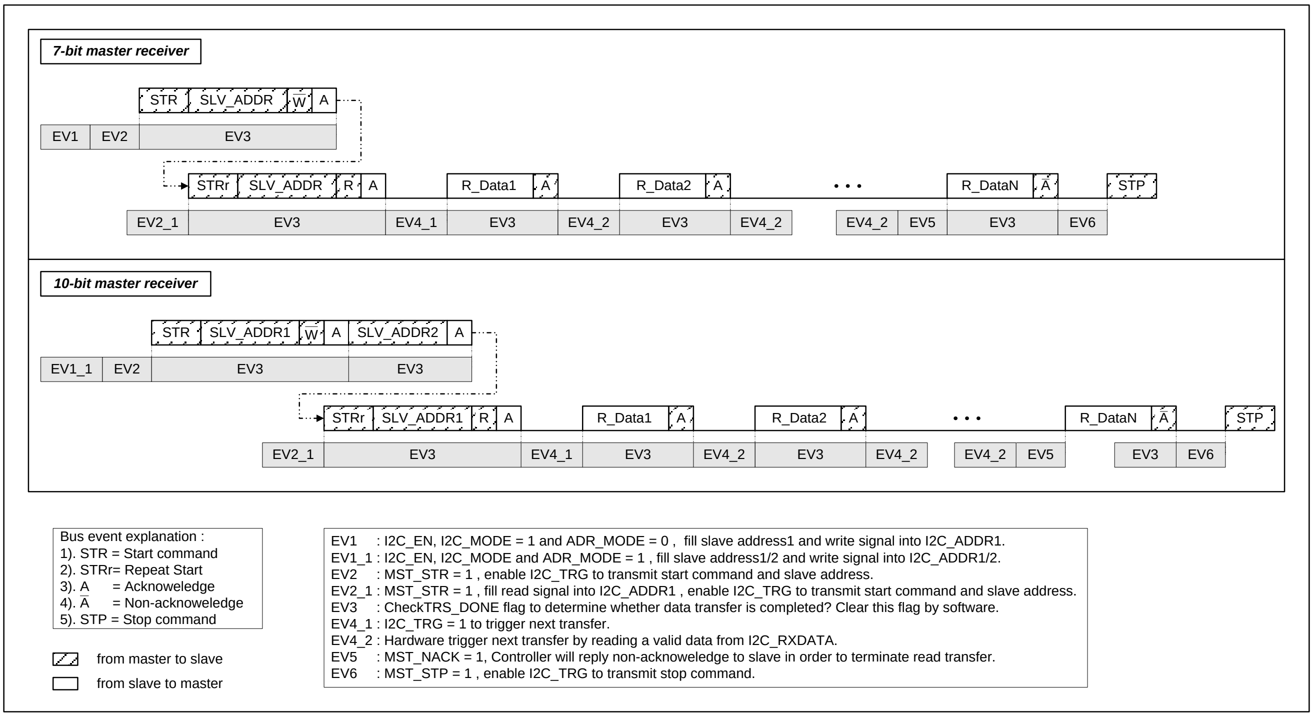


Figure 5-67 I2C transfer bus diagram for master receiver

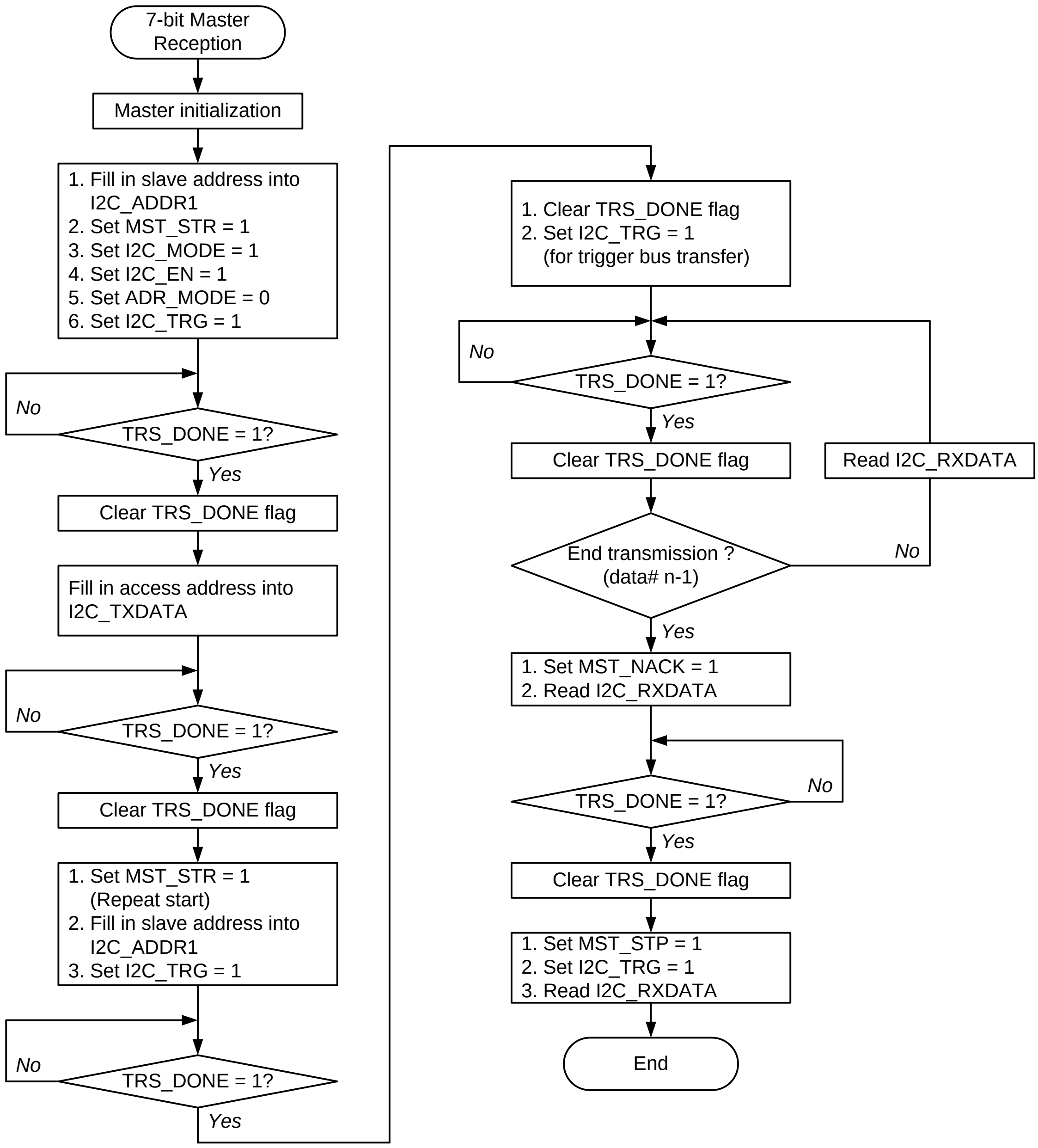


Figure 5-68 I2C transfer sequence flowchart for master receiver (7-bit mode)

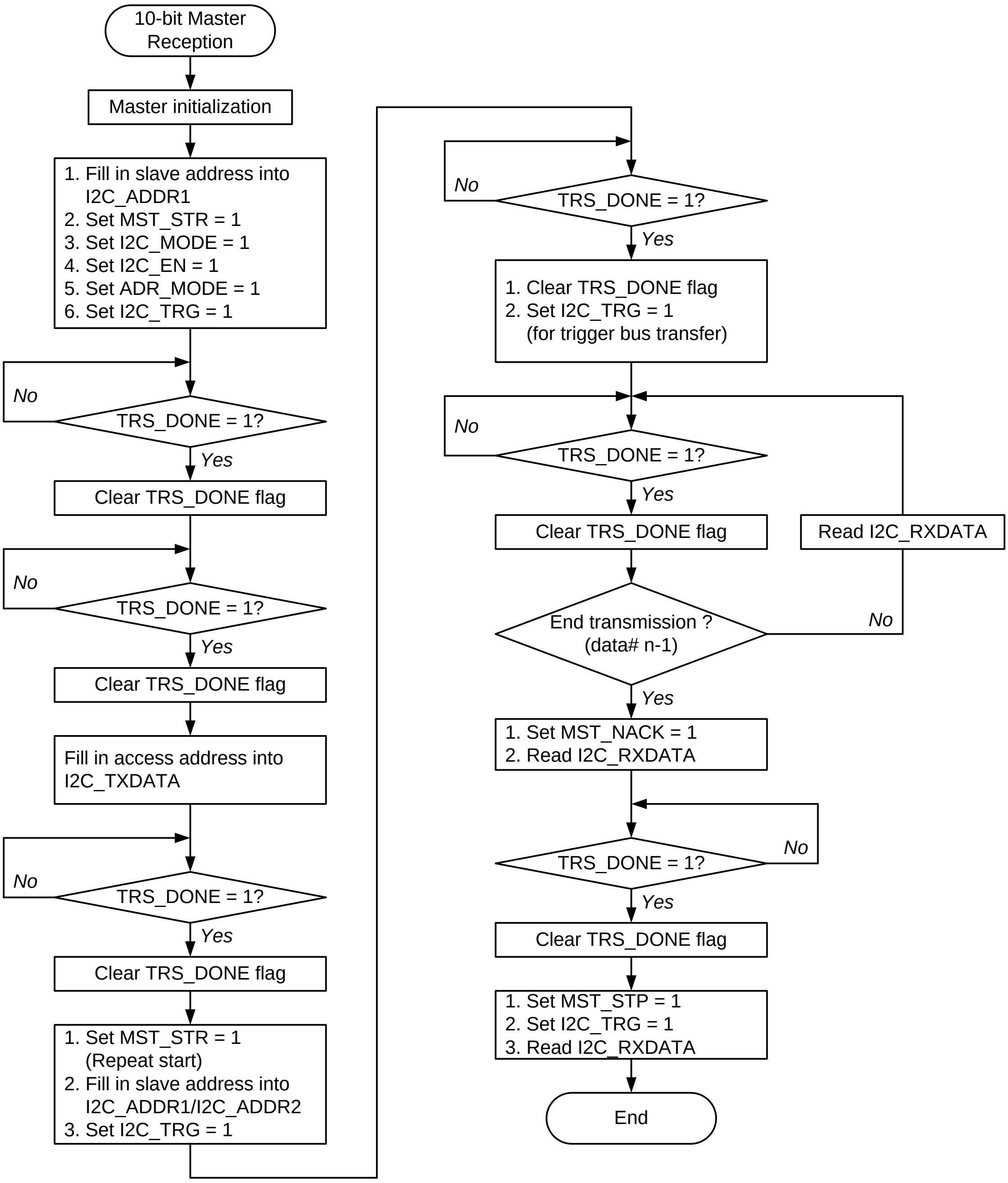


Figure 5-69 I2C transfer sequence flowchart for master receiver (10-bit mode)

5.13.5 Slave Mode

5.13.5.1 General Call

In I2C bus, a 'general call' address which can address all devices. All devices should respond acknowledge when this address is used. However, devices can be made to ignore this address. The **I2C_STS1.GEN_CALL** will be set when slave received a general call. CPU can receive an interrupt request if **I2C_CTRL1.I2C_INTE** is set to 1.

5.13.5.2 I2C slave transmitter

In slave transmitter mode, user must fill slave-address into **I2C_ADDR1/2** and set **I2C_CTRL0.I2C_EN** to 1 before executing data transition. Slave controller will set **I2C_STS0.SLV_ADR_OK** flag to 1 after slave address was received. If the received slave address match to **I2C_ADDR1/2**, **I2C_STS1.SLV_ADR_ERR** is set to 0. Otherwise **I2C_STS1.SLV_ADR_ERR** flag will be set to 1. After checking the slave-address, fill transfer data into **I2C_TXDATA** and starts to transmit data to the master. Once the data is transmitted, the **I2C_STS0.TRS_DONE** and

I2C_STS0.SLV_DAT_OK flag will be set to 1. User must clear these flags by software. Next, fill the latest data into **I2C_TXDATA**. The transfer will be executed until a non-acknowledge and stop command are received.

- SCL clock stretch off :

  In this mode, the SCL clock is not stretched while a packet transfer finished. The transfer data must be filled in **I2C_TXDATA** before SCL clock arrives. Otherwise URON flag will be set to 1.

Below figures show the transfer bus diagram and transfer sequence flowchart for slave transmitter.

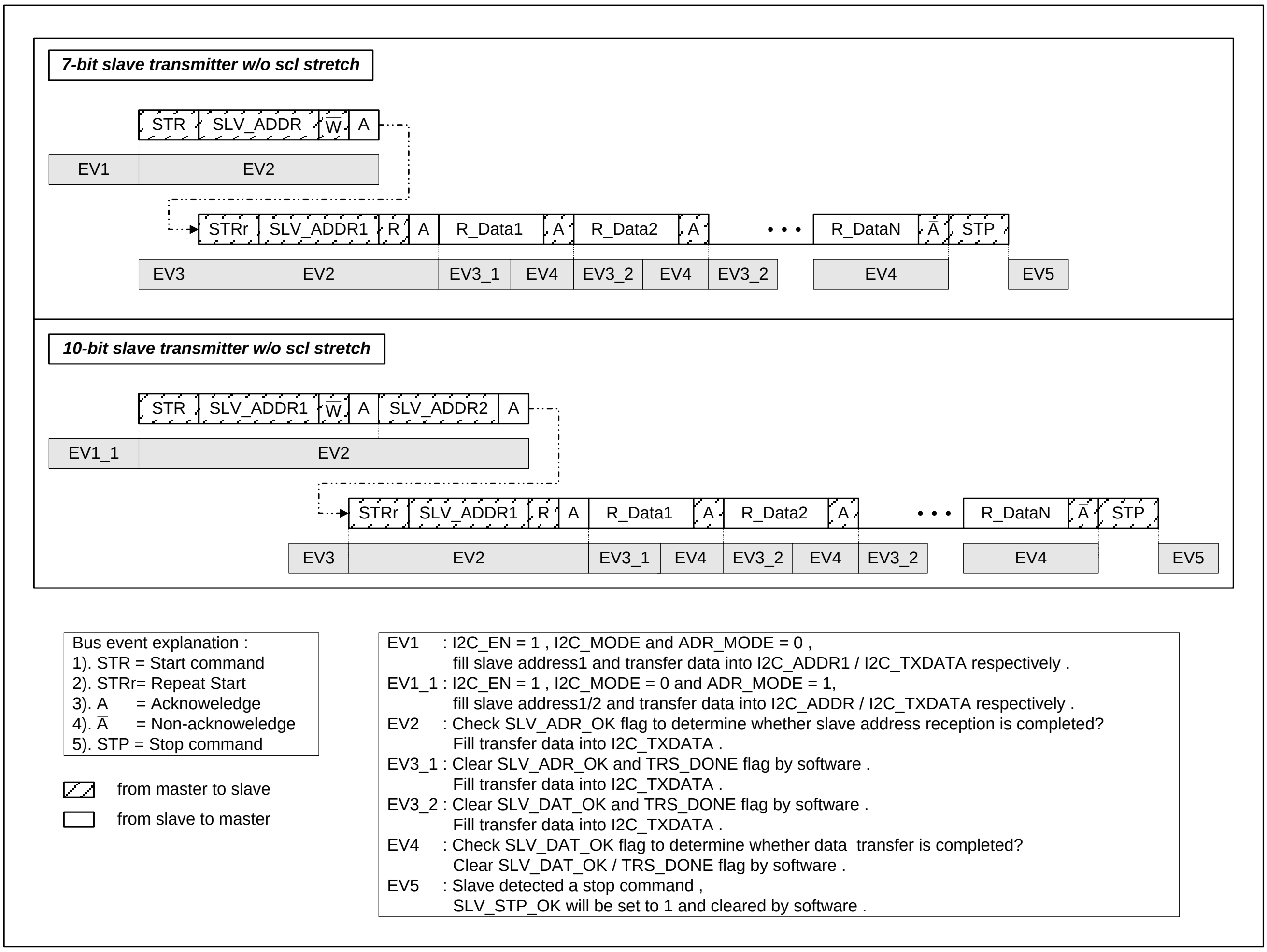


Figure 5-70 I2C transfer bus diagram for slave transmitter (w/o SCL stretch)

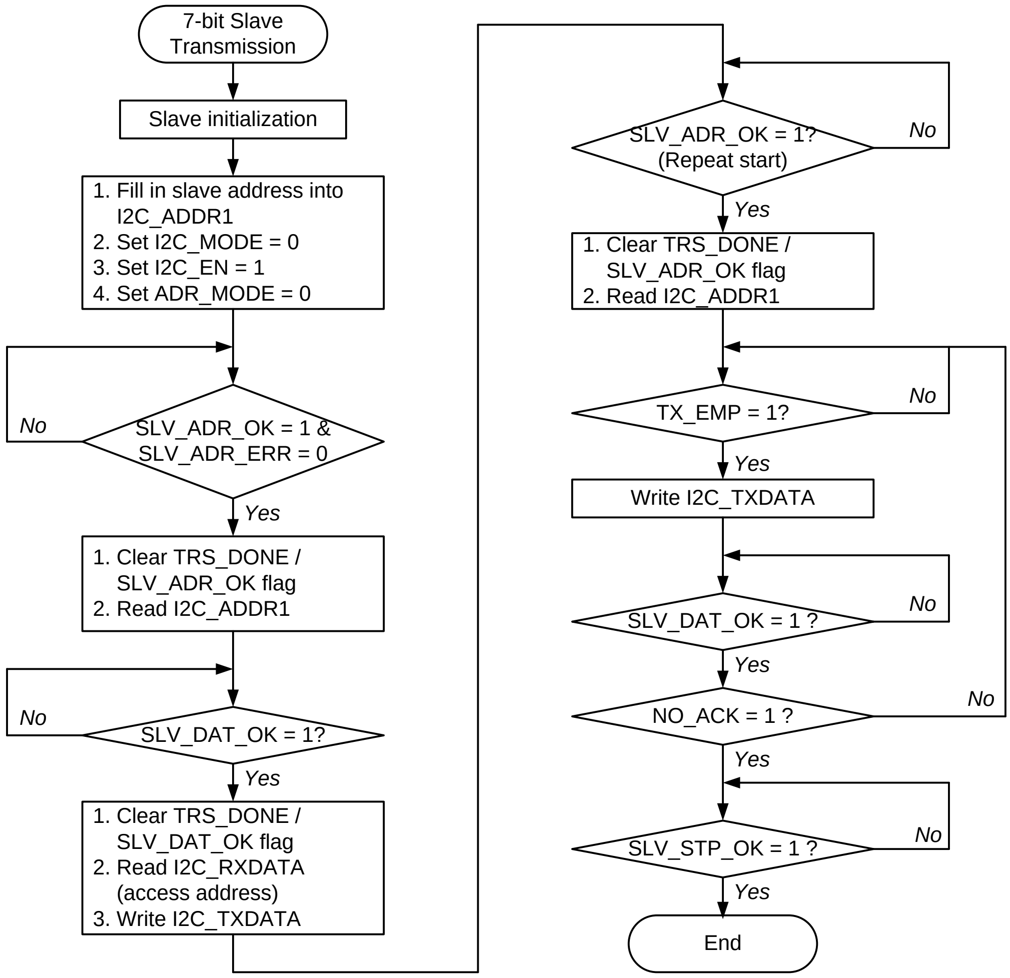


Figure 5-71 I2C transfer sequence flowchart for slave transmitter (7-bit mode w/o SCL stretch)

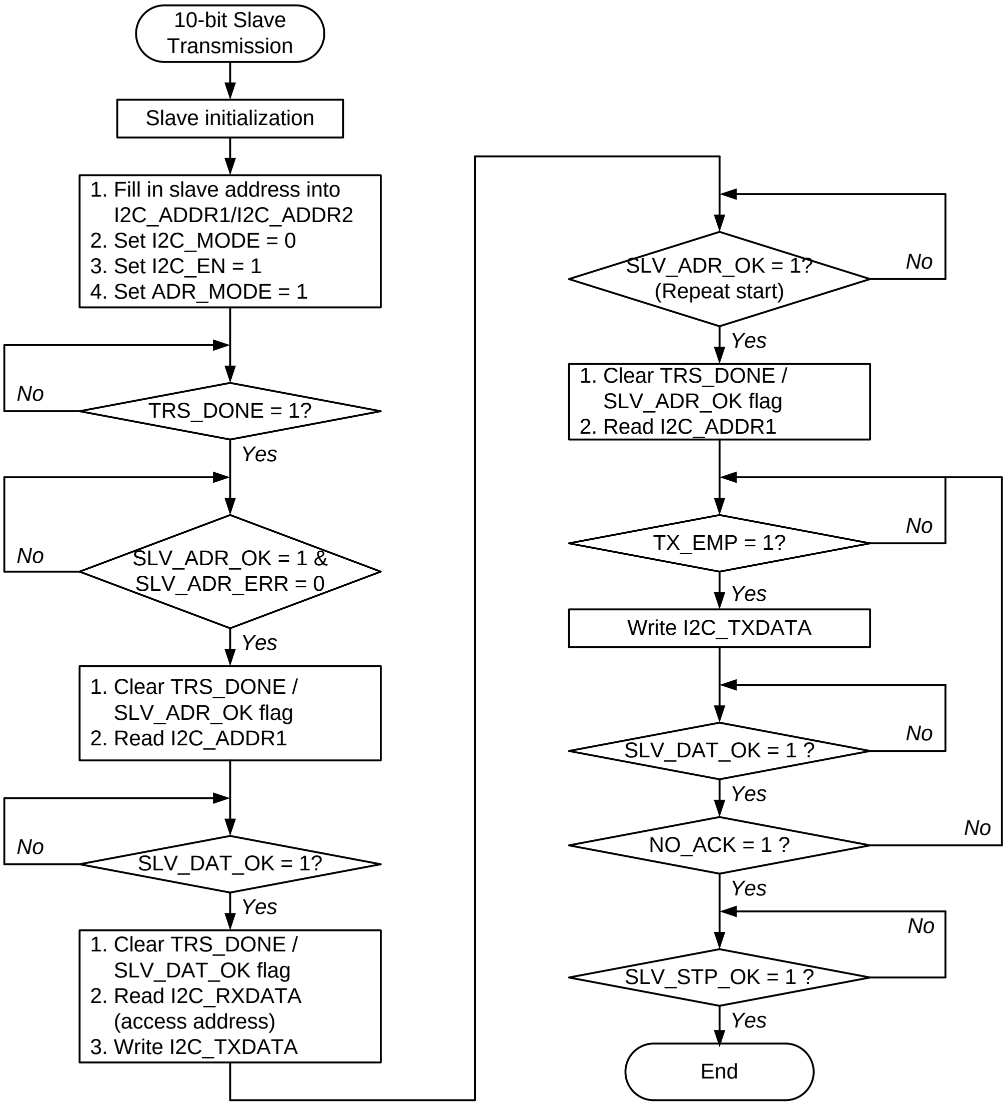


Figure 5-72 I2C transfer sequence flowchart for slave transmitter (10-bit mode w/o SCL stretch)

- SCL clock stretch on:

  In this mode, the SCL clock will be stretched while a packet transfer finished. Slave stretch SCL to low until a new data is filled in **I2C_TXDATA**.

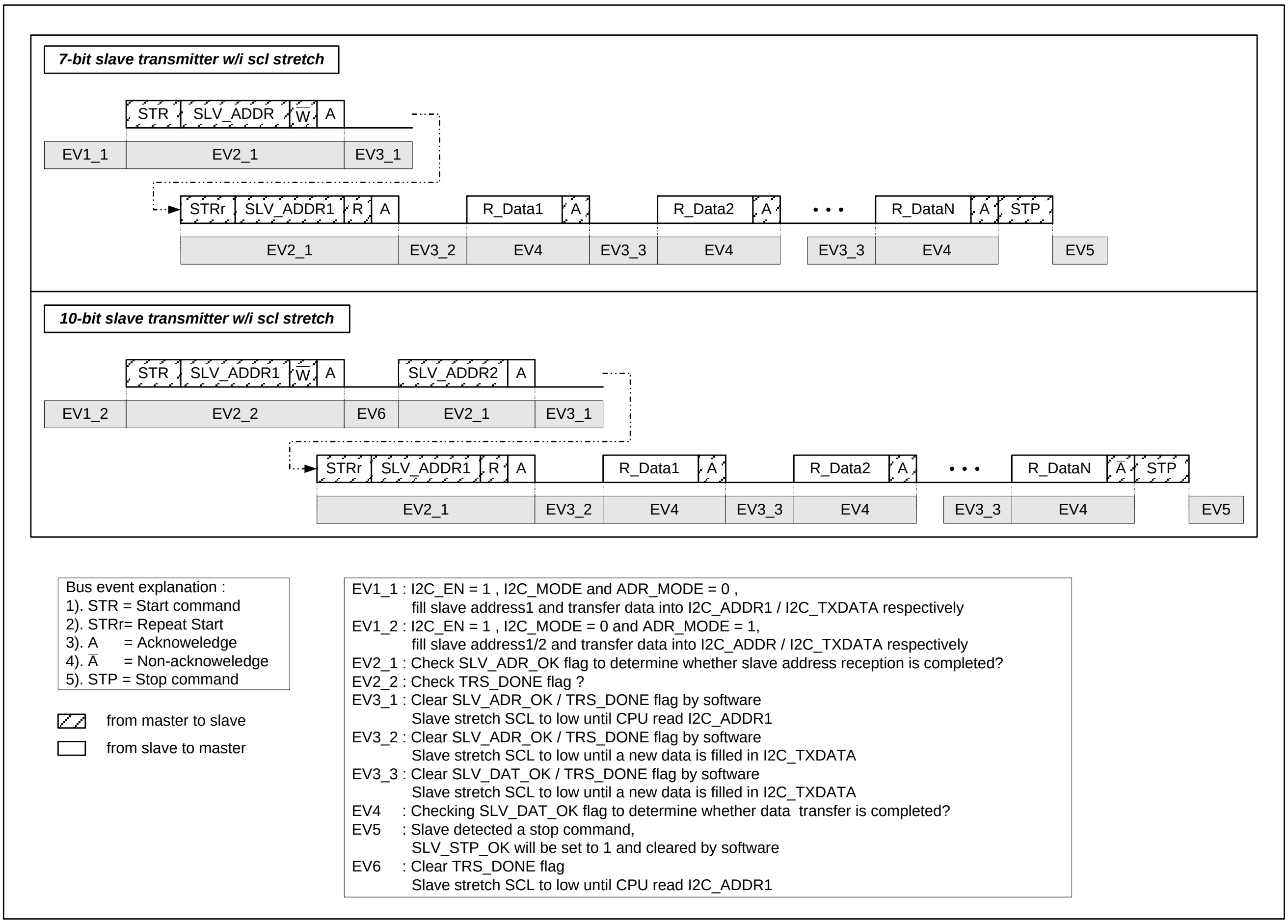


Figure 5-73 I2C transfer bus diagram for slave transmitter (w/i SCL stretch)

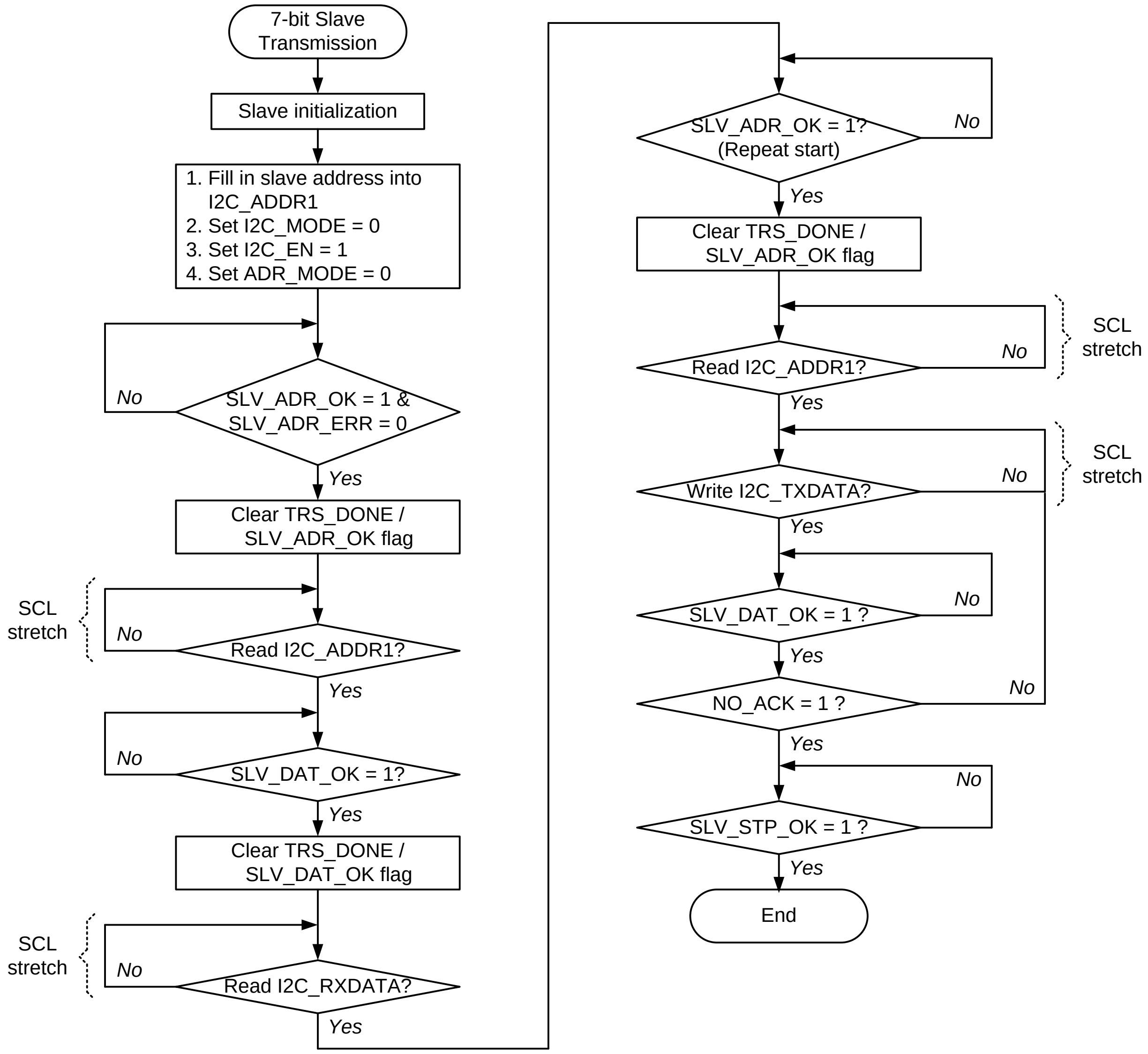


Figure 5-74 I2C transfer sequence flowchart for slave transmitter (7-bit mode w/i SCL stretch)

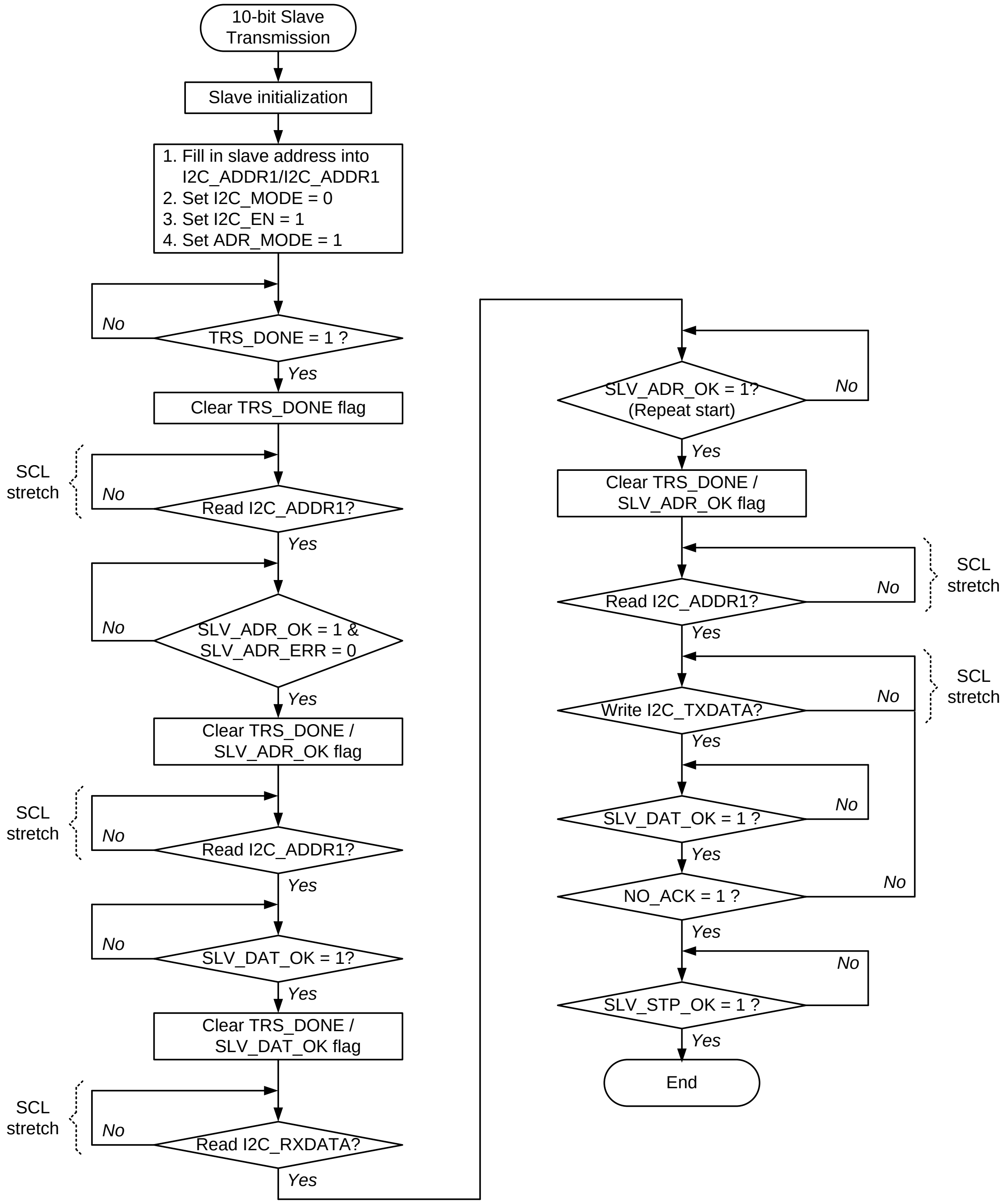


Figure 5-75 I2C transfer sequence flowchart for slave transmitter (10-bit mode w/i SCL stretch)

5.13.5.3 I2C slave receiver

In slave receiver mode, before receiving data from master, user must fill slave-address into **I2C_ADDR1/2** and set **I2C_CTRL0.I2C_EN** to 1. Slave controller will set **I2C_STS0.SLV_ADR_OK** flag to 1 after slave address packet was received. If the received data of slave address matched to **I2C_ADDR1/2**, **I2C_STS1.SLV_ADR_ERR** is set to 0. Otherwise **I2C_STS1.SLV_ADR_ERR** flag will be set to 1. After checking the slave-address, slave controller starts to receive input data from the master. Once the data is received, the **I2C_STS0.TRS_DONE** and **I2C_STS0.SLV_DAT_OK** flag will be set to 1. User must clear these flags by software. Next, read the received data from **I2C_RXDATA**. The transfer will be executed until a stop command is received.

- ❑ SCL clock stretch off :

  In this mode, the SCL clock is not stretched while a packet transfer finished. The transfer data must be read from **I2C_RXDATA** before SCL clock arrives. Otherwise ORON flag will be set to 1.

Below figures show the transfer bus diagram and transfer sequence flowchart for slave receiver.

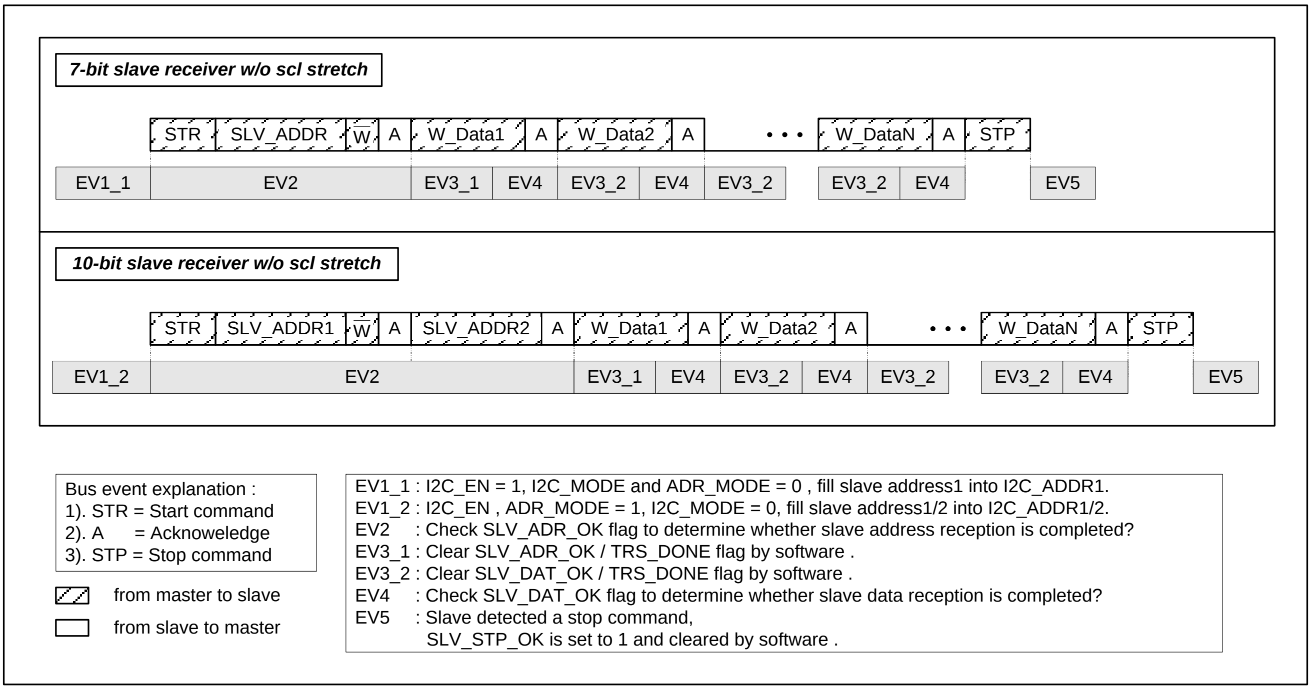


Figure 5-76 I2C transfer bus diagram for slave receiver (w/o SCL stretch)

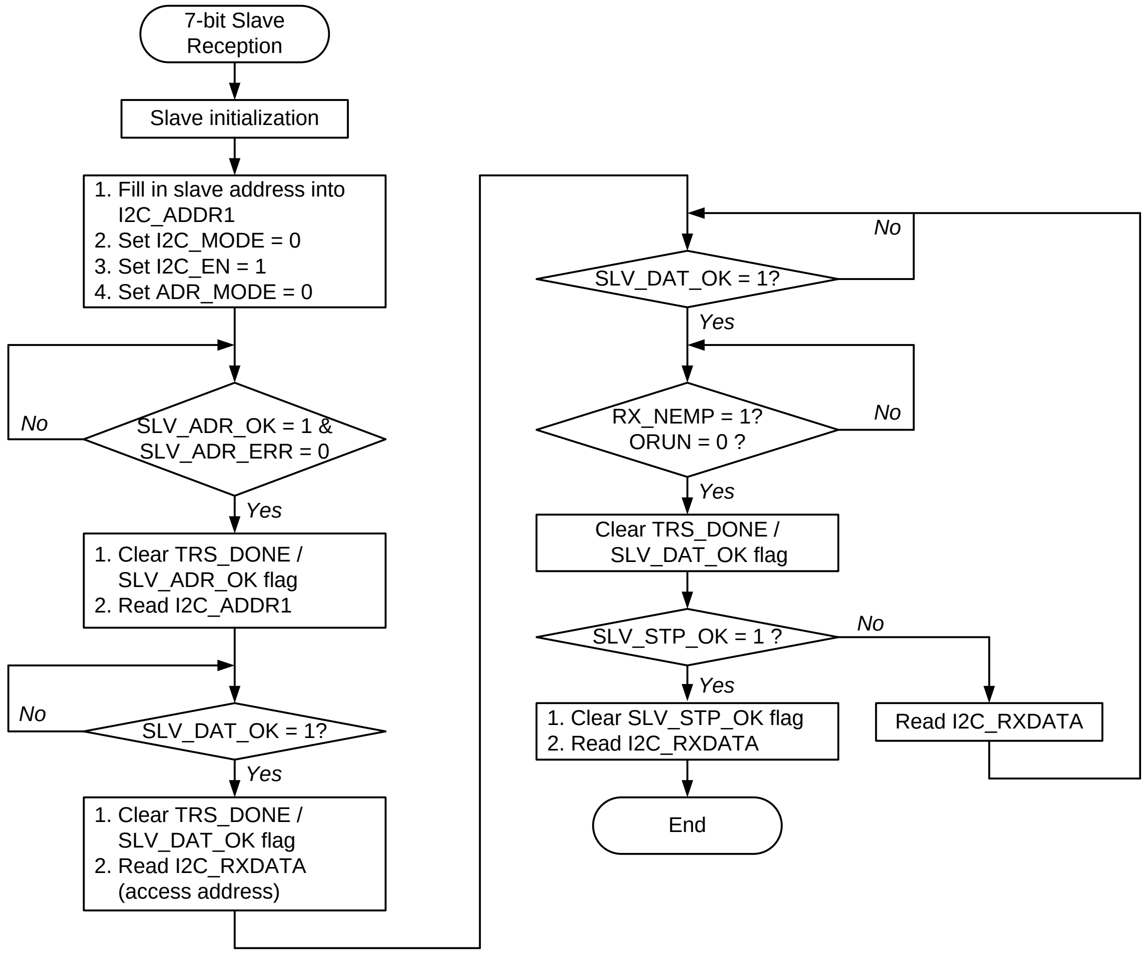


Figure 5-77 I2C transfer sequence flowchart for slave receiver (7-bit mode w/o SCL stretch)

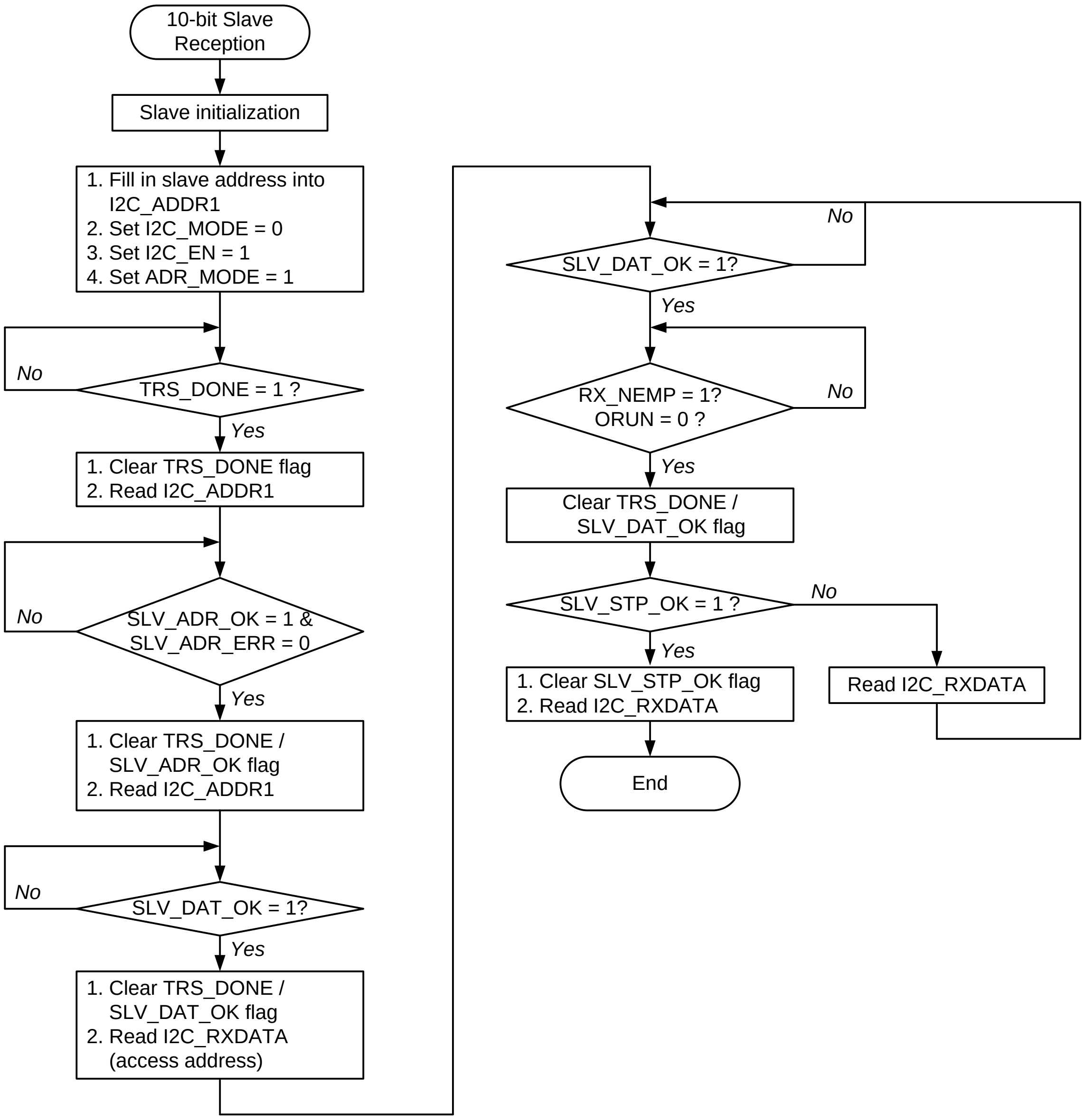


Figure 5-78 I2C transfer sequence flowchart for slave receiver (10-bit mode w/o SCL stretch)

❑ SCL clock stretch on:

In this mode, the SCL clock will be stretched while a packet transfer finished. Slave stretch SCL to low until received data is read from **I2C_RXDATA**.

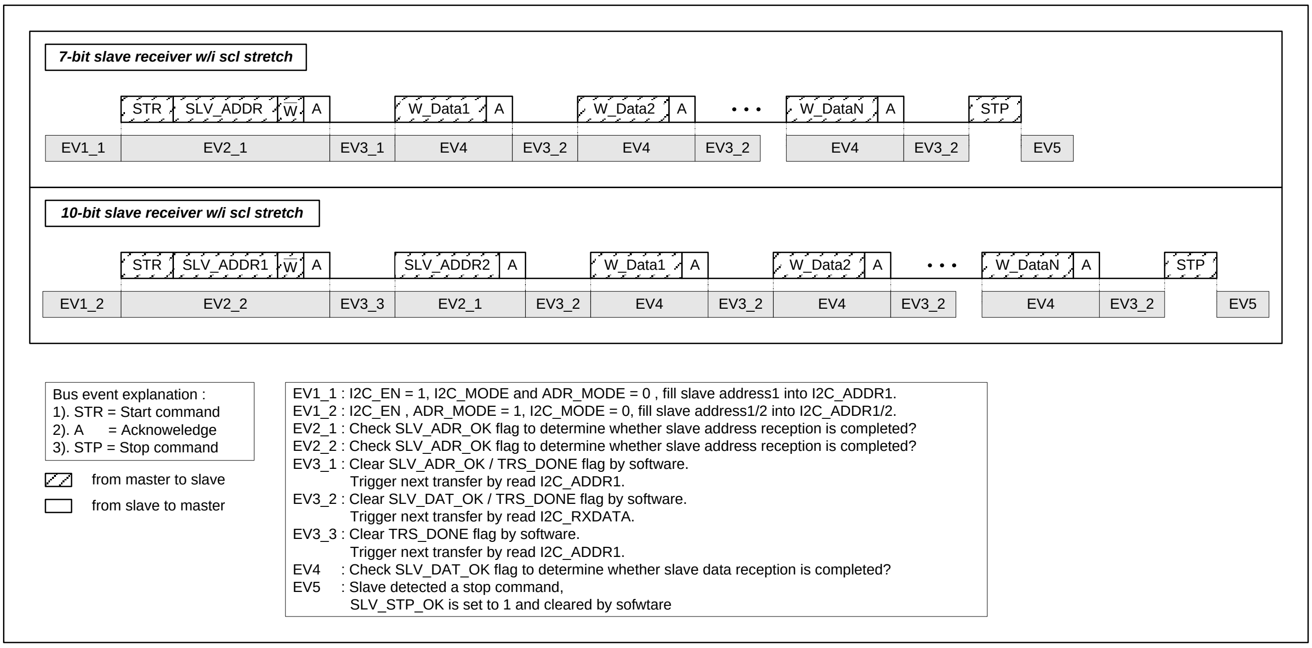


Figure 5-79 I2C transfer bus diagram for slave receiver (w/i SCL stretch)

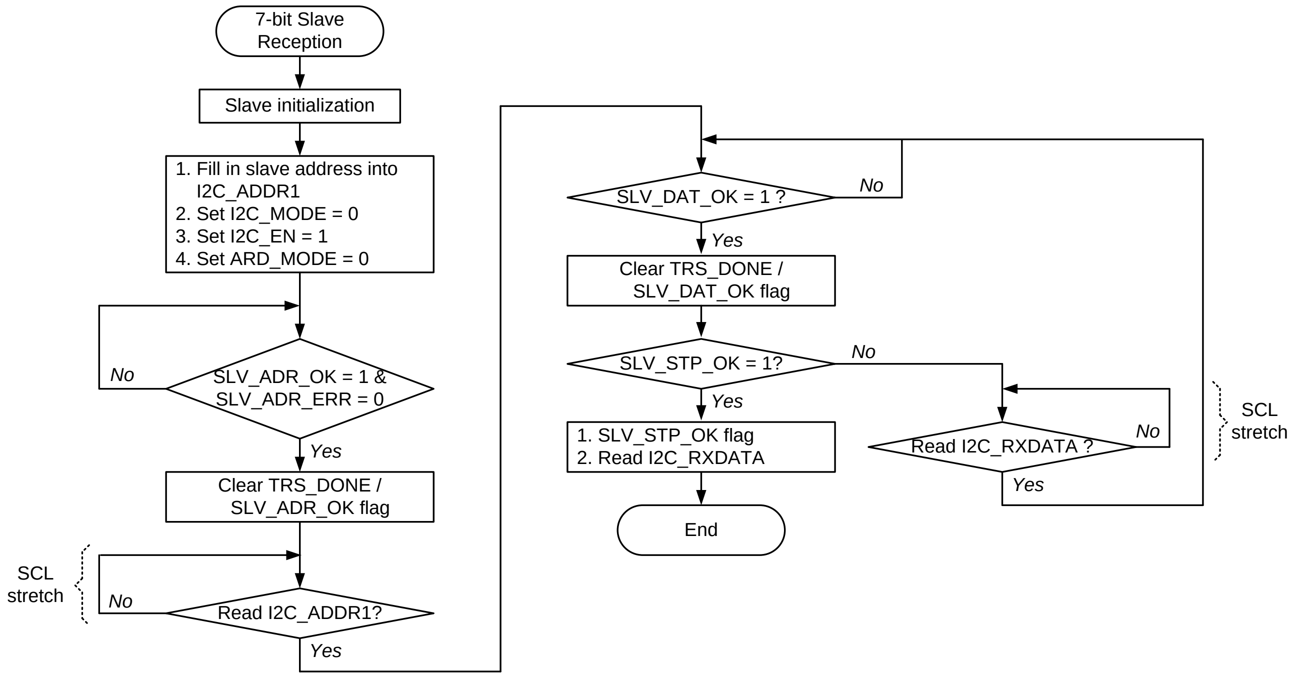


Figure 5-80 I2C transfer sequence flowchart for slave receiver (7-bit mode w/i SCL stretch)

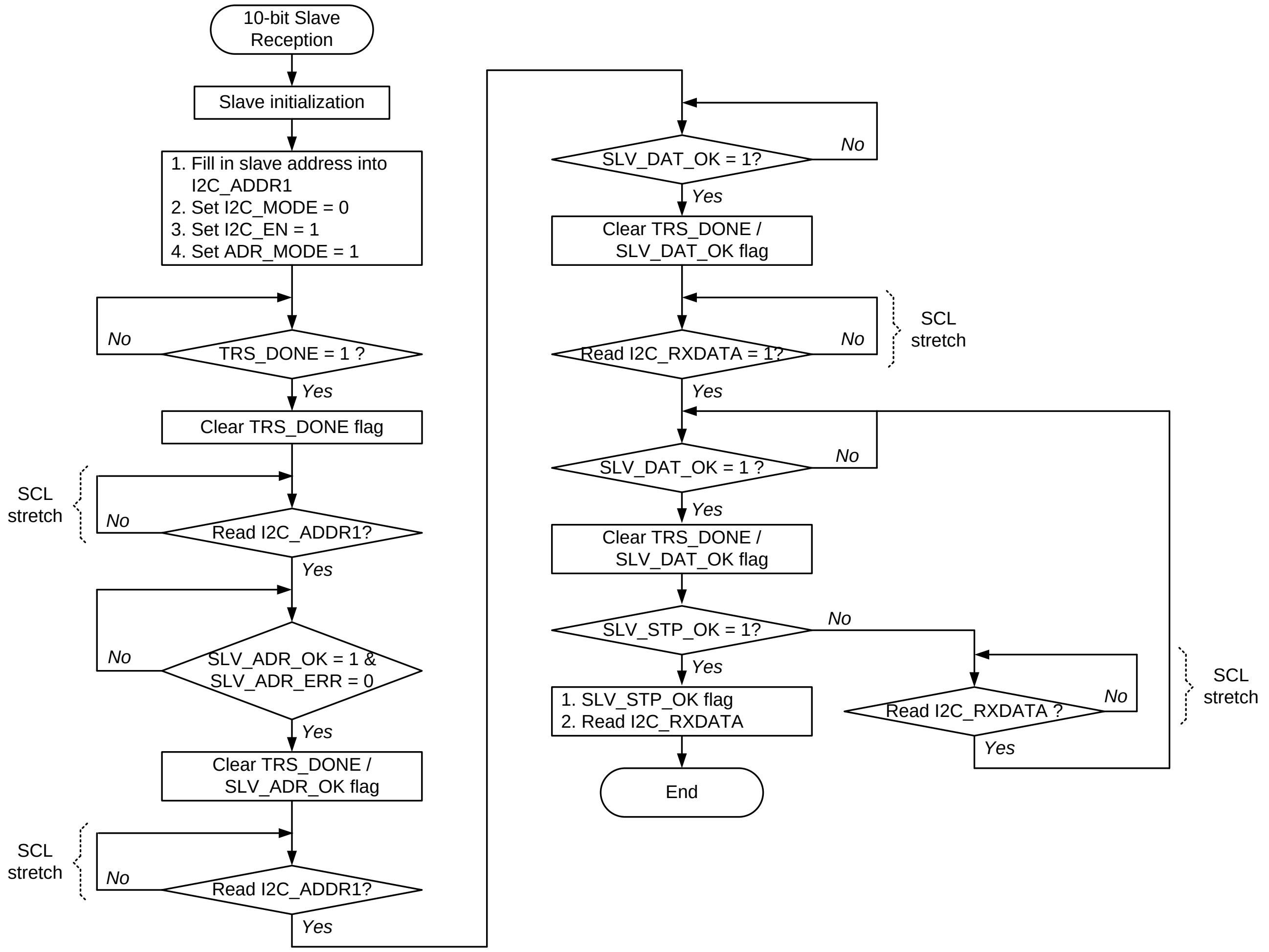


Figure 5-81 I2C transfer sequence flowchart for slave receiver (10-bit mode w/i SCL stretch)

5.13.6 I2C Related Register

I2C_CTRL0			Page: 0 / Address: 0xD9		I2C Control Register0			
Bit	7	6	5	4	3	2	1	0
Function	MST_STR	MST_STP	MST_NACK	I2C_MODE	I2C_CK_SEL		I2C_TRG	I2C_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	MST_STR	R/W	**I2C controller issued start command enable bit** 0 = Disabled 1 = Enabled **Note:** This bit is used in mater only, it will be cleared automatically when current transfer finished.	
6	MST_STP	R/W	**I2C controller issued stop command enable bit** 0 = Disabled 1 = Enabled **Note:** This bit is used in mater only, it will be cleared automatically when current transfer finished.	
5	MST_NACK	R/W	**I2C controller issued non-acknowledge enable bit** 0 = Disabled 1 = Enabled **Note:** This bit is used in mater only, it will be cleared automatically when current transfer finished.	
4	I2C_MODE	R/W	**I2C controller operating mode select bits** 0 = Slave mode 1 = Master mode	
3:2	I2C_CK_SEL	R/W	**I2C controller serial clock select bits** I2C_CK_SEL[1:0] : Clock Source 00 : I2C clock is system clock / 128 01 : I2C clock is system clock / 256 10 : I2C clock is system clock / 768 11 : I2C clock is system clock / 1024	
1	I2C_TRG	R/W	**The start transmission trigger bit** This bit is for master mode only. The I2C master will begin to transmit or receive data when I2C_TRG is set to 1. This bit will be cleared by H/W automatically. 0 = Disabled 1 = Enabled **Note:** This bit is available when I2C_CTRL0.I2C_EN is enabled.	
0	I2C_EN	R/W	**I2C controller enable** 0 = Disabled 1 = Enabled **Note:** This bit must be set to 1 before starting I2C transfer.	

Table 5-204 I2C_CTRL0 register

I2C_CTRL1			**Page: 0 / Address: 0xDA**		**I2C Control Register1**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	SCL_STH_EN	ADR_MODE	ERR_SADR_IE	I2C_INTE
Default	0	0	0	0	1	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
3	SCL_STH_EN	R/W	**SCL stretch enable bit** 0 = Disabled 1 = Enabled (default) **Note:** This bit is available in slave mode only.	
2	ADR_MODE	R/W	**Address mode control bit** 0 = 7-bit mode 1 = 10-bit mode **Note:** This bit is available in slave mode only.	
1	ERR_SADR_IE	R/W	**Slave address error interrupt enable bit** 0 = Disabled 1 = Enabled **Note:** This bit is available in slave mode only.	
0	I2C_INTE	R/W	**I2C interrupt enable bit** 0 = Disabled 1 = Enabled	

Table 5-205 I2C_CTRL1 register

I2C_DBT			**Page: 0 / Address: 0xDB**		**I2C De-bounce Time/ Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	I2C_DB_TIME [5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	0
5:0	I2C_DB_TIME	R/W	**SCL / SDA input de-bounce time** I2C De-bounce time is the set value of I2Cx_CTRL.I2C_DB_TIME plus one. **Note:** The counting clock is PCLK	

Table 5-206 I2C_DEBOUNCE register

I2C_STS0			**Page: 0 / Address: 0xDC**		**I2C Status Register0**			
Bit	7	6	5	4	3	2	1	0
Function	RX_NEMP	TX_EMP	ARB_LOST	SLV_ADR_OK	SLV_DAT_OK	SLV_STP_OK	NO_ACK	TRS_DONE
Default	0	1	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RX_NEMP	R	**I2C Rx buffer is not empty flag** Read: 0 = I2C Rx buffer is empty	

Bit	Function	Type	Description	Condition
			1 = I2C Rx buffer is not empty	
6	TX_EMP	R/W	**I2C Tx buffer is empty flag** Read: 0 = I2C Tx buffer is not empty 1 = I2C Tx buffer is empty	
5	ARB_LOST	R/W	**I2C bus arbitration lost flag** Read: 0 = I2C bus arbitration lost is not occurred 1 = I2C bus arbitration lost is occurred Write: 0 = Clear this bit 1 = No effect **Note:** This error occurs when the I2C interface detects an arbitration lost condition. It is available in master mode only.	
4	SLV_ADR_OK	R/W	**Slaved address had been received** Read: 0 = Slave address is not asserted 1 = Slave address is asserted and match to the setting Write: 0 = Clear this bit 1 = No effect **Note:** This bit is available in slave mode only.	
3	SLV_DAT_OK	R/W	**Data transmit or receive done flag** Read: 0 = Data is transmitting or idle now 1 = Data is transmission complete Write: 0 = Clear this bit 1 = No effect **Note:** This bit is available in slave mode only.	
2	SLV_STP_OK	R/W	**Stop command had received flag** Read: 0 = Stop command is not be received 1 = Stop command had received Write: 0 = Clear this bit 1 = No effect **Note:** This bit is available in slave mode only.	
1	NO_ACK	R/W	**I2C have not received acknowledging signal.** Read : 0 = Acknowledge 1 = No acknowledge Write: 0 = Clear this bit 1 = No effect	
0	TRS_DONE	R/W	**I2C controller transmission complete flag** Read:	

Bit	Function	Type	Description	Condition
			0 = I2C is idle or on going 1 = I2C finished data transmission Write: 0 = Clear this bit 1 = No effect	

Table 5-207 I2C_STS0 register

I2C_STS1				**Page: 0 / Address: 0xDD**		**I2C Status Register1**		
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	URUN	ORUN	SLV_ADR_ERR	BUSY	GEN_CALL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	URUN	R/W	**I2C under run flag** 0 = I2C is not under run 1 = I2C is under run **Note:** This bit is available in slave mode only	
3	ORUN	R/W	**I2C over run flag** 0 = I2C is not over run 1 = I2C is over run **Note:** This bit is available in slave mode only	
2	SLV_ADR_ERR	R/W	**Slave address error flag** Read: 0 = Slave address is correct address 1 = Slave address is wrong address Write: 0 = Clear this bit 1 = No effect **Note:** This bit is available in slave mode only.	
1	BUSY	R/W	**I2C controller busy flag** Read: 0 = No communication on the bus 1 = Communication ongoing on the bus Write: 0 = Clear this bit 1 = No effect	
0	GEN_CALL	R/W	**I2C general call flag** Read: 0 = I2C master has issued general call 1 = I2C master has not issued general call Write: 0 = Clear this bit 1 = No effect	

Table 5-208 I2C_STS1 register

I2C_ADDR1			Page: 0 / Address: 0xE1		I2C Address Register			
Bit	7	6	5	4	3	2	1	0
Function	**ADDR1[6:0]**							R_W
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	ADDR1[6:0]	R/W	**Address 1st 7Bits** 7-bit addressing mode : ADDR1[6:0] = slave address[6:0] 10-bit addressing mode: ADDR1[6:2] = 0x1E ; ADDR1[1:0] = slave address[9:8]	
0	R_W	R/W	**I2C read / write control signal** 0 = Write 1 = Read **Note:** This bit is shared between master and slave mode.	

Table 5-209 I2C_ADDR0 register

I2C_ADDR2			Page: 0 / Address: 0xE2		I2C Address Register			
Bit	7	6	5	4	3	2	1	0
Function	**ADDR2**							
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:0	ADDR2	R/W	**Address 2nd Byte** 7-bit addressing mode : none 10-bit addressing mode: slave address[7:0]	

Table 5-210 I2C_ADDR1 register

I2C_TXDATA			Page: 0 / Address: 0xE3		I2C Transmit Data Register			
Bit	7	6	5	4	3	2	1	0
Function	I2C_TXDATA[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	I2C_TXDATA	R/W	**I2C transmit data register.** **Note:** This register is shared between master and slave mode.	

Table 5-211 I2C_TXDATA register

I2C_RXDATA			Page: 0 / Address: 0xE4		I2C Receive Data Register			
Bit	7	6	5	4	3	2	1	0
Function	I2C_RXDATA[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	I2C_RXDATA	R/W	**I2C receive data register.** **Note:** This register is shared between master and slave	

Bit	Function	Type	Description	Condition
			mode.	

Table 5-212 I2C_RXDATA register

5.14. Operating Amplifier and Comparator Unit

The GPM8F3331B has embedded three operating amplifiers and two comparators. To ensure the OP and CMP applications are correct, user must pay attention to the OP/CMP interface state to avoid GPIO influence.

5.14.1. OP0

OP0 has built-in input and feedback resistance path. The OP0_O will be 21 times larger than the OP_P input voltage. In addition, user can set the output voltage clamping action by setting OP_CTRL0. For more flexible application, the output signal of OP0 is connected to CMP0 and a channel of ADC by interconnection. User can use this function by setting the OP_CTRL0 register. When OP0_P_IF_EN and OP0_N_IF_EN are setting, the GPIO (P00 and P01) will be input floating state.

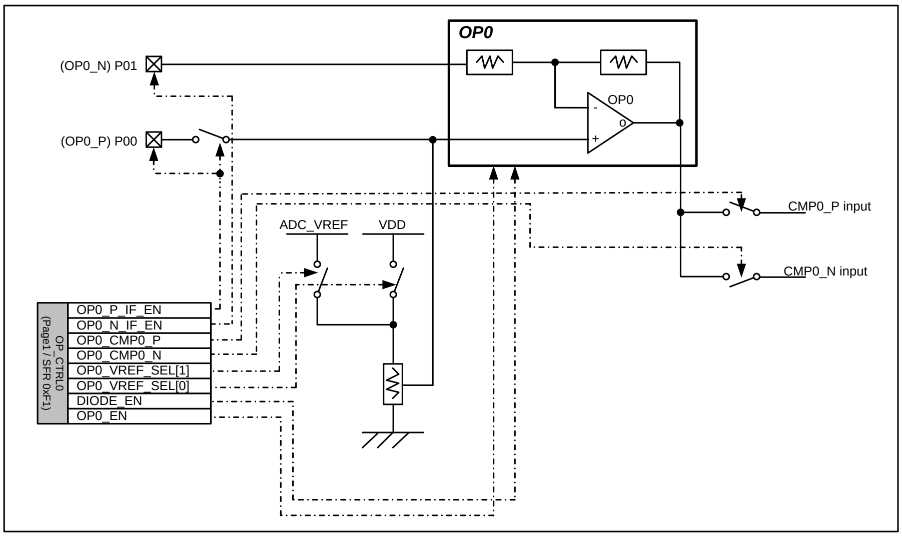


Figure 5-82 OP0 Block Diagram

5.14.2. OP1

The OP1 supports 20/40 gain select for user application. In addition, its output has three connection paths for more flexible functionality for different application. When OP1_P_IF_EN , OP1_CAP_IF_EN and OP1_O_IF_EN are enabled, the GPIO (P11, P10 and P07) will be input floating state.

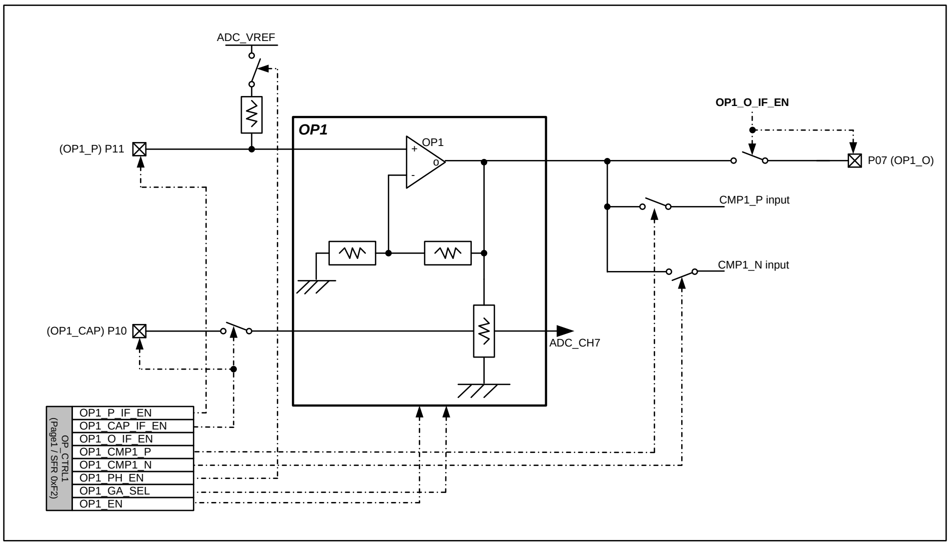


Figure 5-83 OP1 Block Diagram

5.14.3. OP2

The OP2 supports 10/20 gain select for user application. When OP2_N_IF_EN is enabled, the GPIO (P06) will be input floating state.

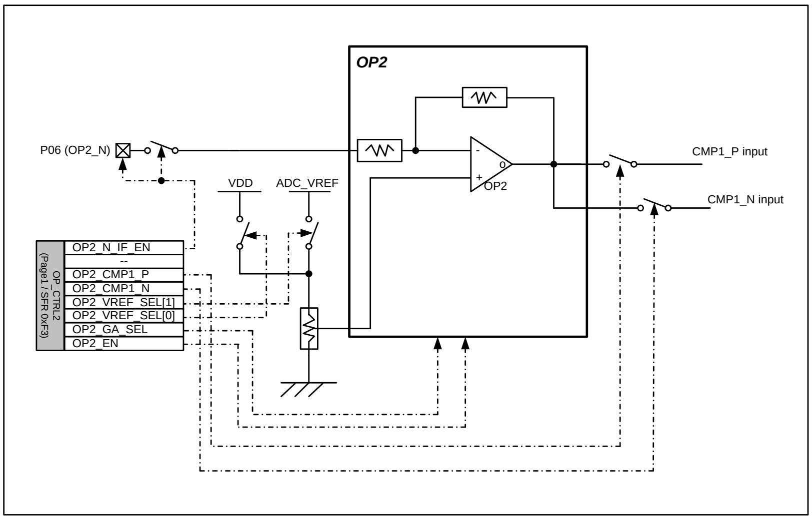


Figure 5-84 OP2 Block Diagram

5.14.4. CMP0 and CMP1

The GPM8F3331B supports two sets analog comparators. They provide an input hysteresis windows and output de-bounce filter to resist noise. When CMP0_P_IF_EN , CMP0_N_IF_EN , CMP1_P_IF_EN and CMP1_N_IF_EN is setting, the GPIO (P02 , P03, P04 and P05) will be input floating state.

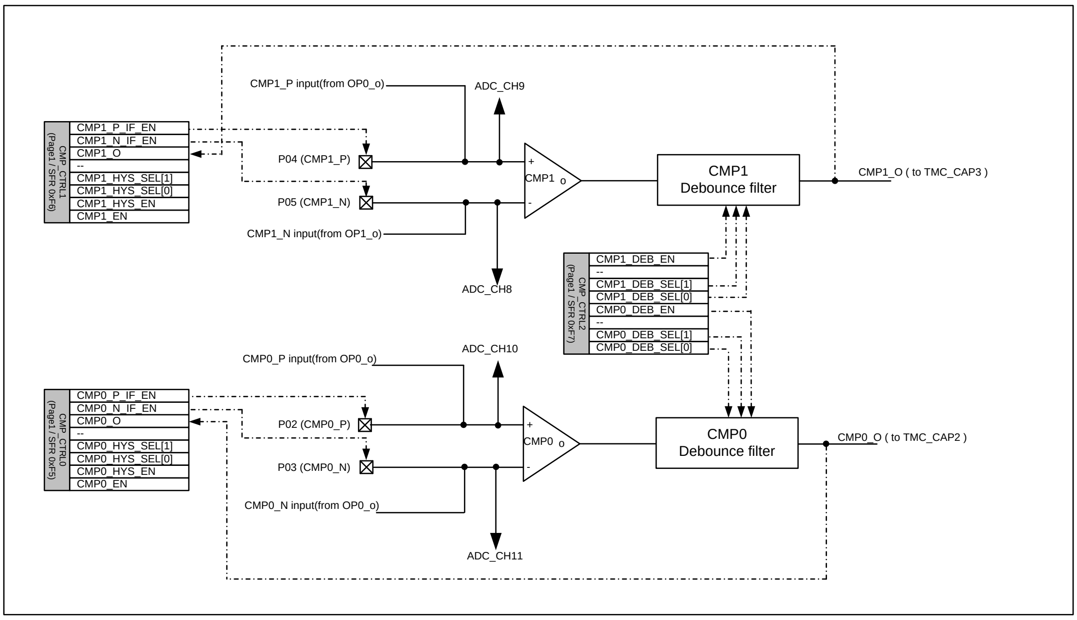


Figure 5-85 CMP0 and CMP1 Block Diagram

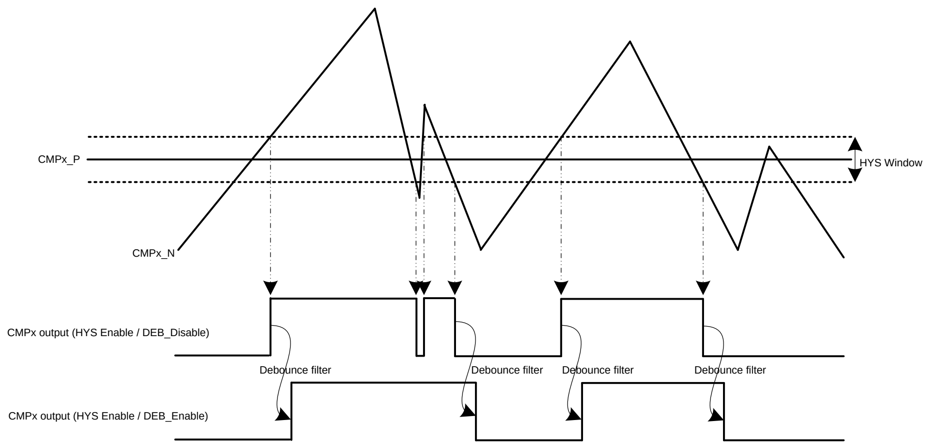


Figure 5-86 Comparator hysteresis function diagram

5.14.5. OP and CMP Related Register

OP_CTRL0			Page: 1 / Address: 0xF1		Operating Amplifier Control Register 0			
Bit	7	6	5	4	3	2	1	0
Function	OP0_P _IF_EN	OP0_N _IF_EN	OP0_ CMP0_P	OP0_ CMP0_N	OP0_VREF_SEL[1:0]		Diode_EN	OP0_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	OP0_P_IF_EN	R/W	OP0 Positive interface enable. 0: Disabled 1: Enabled When this bit is enabled, the P00 will be input floating state.	

Bit	Function	Type	Description	Condition
6	OP0_N_IF_EN	R/W	OP0 Negative interface enable 0: Disabled 1: Enabled When this bit is enabled, the P01 will be input floating state.	
5	OP0_CMP0_P	R/W	OP0 output to CMP0 Positive input switch enable 0: Disabled 1: Enabled	
4	OP0_CMP0_N	R/W	OP0 output to CMP0 Negative input switch enable 0: Disabled 1: Enabled	
3:2	OP0_VREF_SEL	R/W	OP0 Positive reference voltage source 00: Disabled 01: From VDD 10: From ADC_VREF 11: Prohibited	
1	Diode_EN	R/W	OP0 Feedback clamp diode enable 0: Disabled 1: Enabled	
0	OP0_EN	R/W	OP0 enable control signal 0: Disabled 1: Enabled	

Table 5-213 OP_CTRL0 register

OP_CTRL1			Page: 1 / Address: 0xF2		Operating Amplifier Control Register 1			
Bit	7	6	5	4	3	2	1	0
Function	OP1_P_IF_EN	OP1_CAP_IF_EN	OP1_O_IF_EN	OP1_CMP1_P	OP1_CMP1_N	OP1_PH_EN	OP1_GA_SEL	OP1_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	OP1_P_IF_EN	R/W	OP1 Positive interface enable 0: Disabled 1: Enabled When this bit is enabled, the P11 will be input floating state.	
6	OP1_CAP_IF_EN	R/W	OP1 Cap path interface enable 0: Disabled 1: Enabled When this bit is enabled, the P10 will be input floating state.	
5	OP1_O_IF_EN	R/W	OP1 output interface enable 0: Disabled 1: Enable When this bit is enabled, the P07 will be input floating state.	
4	OP1_CMP1_P	R/W	OP1 output to CMP1 Positive input switch enable 0: Disabled 1: Enabled	
3	OP1_CMP1_N	R/W	OP1 output to CMP1 Negative input switch enable 0: Disabled 1: Enabled	

Bit	Function	Type	Description	Condition
2	OP1_PH_EN	R/W	OP1 positive pull high enable 0: Disabled 1: Enabled	
1	OP1_GA_SEL	R/W	OP1 gain select 0: 20 gain 1: 40 gain	
0	OP1_EN	R/W	OP1 enable control signal 0: Disabled 1: Enabled	

Table 5-214 OP_CTRL1 register

OP_CTRL2			Page: 1 / Address: 0xF3		Operating Amplifier Control Register 2			
Bit	7	6	5	4	3	2	1	0
Function	OP2_N_IF_EN	--	OP2_CMP1_P	OP2_CMP1_N	OP2_VREF_SEL[1:0]		OP2_GA_SEL	OP2_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	OP2_N_IF_EN	R/W	OP2 Negative interface enable 0: Disabled 1: Enabled When this bit is enabled, the P06 will be input floating state.	
6	--	R/W	Reserved	
5	OP2_CMP1_P	R/W	OP2 output to CMP1 Positive input switch enable 0: Disabled 1: Enabled	
4	OP2_CMP1_N	R/W	OP2output to CMP1 Negative input switch enable 0: Disabled 1: Enabled	
3:2	OP2_VREF_SEL	R/W	OP2 Positive reference voltage source 00: Disabled 01: From VDD 10: From ADC_VREF 11: Prohibited	
1	OP2_GA_SEL	R/W	OP2 gain select 0: 20 gain 1: 10 gain	
0	OP2_EN	R/W	OP2 enable control signal 0: Disabled 1: Enabled	

Table 5-215 OP_CTRL2 register

CMP_CTRL0			Page: 1 / Address: 0xF5		Comparator Control Register 0			
Bit	7	6	5	4	3	2	1	0
Function	CMP0_P_IF_EN	CMP0_N_IF_EN	CMP0_O	--	CMP0_HYS_SEL		CMP0_HYS_EN	CMP0_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CMP0_P_IF_EN	R/W	CMP0 Positive interface enable 0: Disabled 1: Enabled When this bit is enabled, the P02 will be comparator 0 positive input port	
6	CMP0_N_IF_EN	R/W	CMP0 Negative interface enable 0: Disabled 1: Enabled When this bit is enabled, the P03 will be comparator 0 negative input port	
5	CMP0_O	R	Comparator 0 output state	
4	--	R/W	Reserved	
3:2	CMP0_HYS_SEL[1:0]	R/W	CMP0 Hysteresis select 00: +/-10mV 01: +/-25mV 10: +/-60mV 11: +/-100mV	
1	CMP0_HYS_EN	R/W	CMP0 Hysteresis window enable 0: Disabled 1: Enabled	
0	CMP0_EN	R/W	CMP0 enable control signal 0: Disabled 1: Enabled	

Table 5-216 CMP_CTRL0 register

CMP_CTRL1			Page: 1 / Address: 0xF6		Comparator Control Register 1			
Bit	7	6	5	4	3	2	1	0
Function	CMP1_P_IF_EN	CMP1_N_IF_EN	CMP1_O	--	CMP1_HYS_SEL		CMP1_HYS_EN	CMP1_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CMP1_P_IF_EN	R/W	CMP1 Positive interface enable 0: Disabled 1: Enabled If this bit set 1 , the P04 will be comparator 1 positive input port	
6	CMP1_N_IF_EN	R/W	CMP1 Negative interface enable 0: Disabled 1: Enabled If this bit set 1 , the P05 will be comparator 1 negative input port	
5	CMP1_O	R	Comparator 1 output state	
4	--	R/W	Reserved	
3:2	CMP1_HYS_SEL[1:0]	R/W	CMP1 Hysteresis select 00: +/-10mV 01: +/-25mV 10: +/-60mV	

Bit	Function	Type	Description	Condition
			11: +/-100mV	
1	CMP1_HYS_EN	R/W	CMP1 Hysteresis window enable 0: Disabled 1: Enabled	
0	CMP1_EN	R/W	CMP1 enable control signal 0: Disabled 1: Enabled	

Table 5-217 CMP_CTRL1 register

CMP_CTRL2			Page: 1 / Address: 0xF7		Comparator Control Register 1			
Bit	7	6	5	4	3	2	1	0
Function	CMP1_DEB_EN	--	CMP1_DEB_SEL		CMP0_DEB_EN	--	CMP0_DEB_SEL	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CMP1_DEB_EN	R/W	CMP1 Debounce Enable 0: Disabled 1: Enabled	
6	--	--	Revised	
5:4	CMP1_DEB_SEL	R/W	CMP1 Debounce Selection 00: 50T system clk 01: 120T system clk 10: 200T system clk 11: 256T system clk	
3	CMP0_DEB_EN	R/W	CMP1 Debounce Enable 0: Disabled 1: Enabled	
2	--	--	Revised	
1:0	CMP0_DEB_SEL	R/W	CMP0 Debounce Selection 00: 50T system clk 01: 120T system clk 10: 200T system clk 11: 256T system clk	

Table 5-218 CMP_CTRL2 register

5.15. IO DC Bias Output

5.15.1. Bias output

GPM8F3331B is equipped with two IOs(P12/P13) that support DC bias voltage output capability. The DC voltage includes DC 3.3V , 0.6V or 0V. Users can use this function by setting SYS_CTRL2.LDO33_EN and Charge_CTRL.IO33V_EN to 1. Then, the P12 and P13 will switch to DC voltage output. For different requirement, user can change different output voltage by setting Charge_CTRL.VOL_P12 and Charge_CTRL.VOL_P13.

5.15.2. Release Register

Charge_CTRL			Page: 1 / Address: 0xFD		Comparator Control Register 0			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	VOL_P13		VOL_P12		IO33V_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:3	VOL_P13	R/W	Control P13 output voltage select (DM) 00: High-Z state 01: 0V 10: 0.6V 11: 3.3V	
2:1	VOL_P12	R/W	Control P12 output voltage select (DP) 00: High-Z state 01: 0V 10: 0.6V 11: 3.3V	
0	IO33V_EN	R/W	Control GPIO P12 and P13 output 3.3V or 0.6V	

Table 5-219 Charge_CTRL register

5.16. Alphabetical List of Instruction Set

5.16.1. Arithmetic Operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
INC DPTR	Increment data pointer	0xA3	1	1

Mnemonic	Description	Code	Bytes	Cycles
MUL A,B	Multiply A and B	0xA4	1	2
DIV A,B	Divide A by B	0x84	1	6
DA A	Decimal adjust accumulator	0xD4	1	3

5.16.2. Logic Operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL direct,A	AND accumulator to direct byte	0x52	2	3
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
XRL A,Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1

5.16.3. Boolean Operations

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
MOV C,bit	Move direct bit to carry flag	0xA2	2	2

Mnemonic	Description	Code	Bytes	Cycles
MOV bit,C	Move carry flag to direct bit	0x92	2	3

5.16.4. Data Transfers

<table>
<tr><th>Mnemonic</th><th colspan="2">Description</th><th>Code</th><th>Bytes</th><th>Cycles</th></tr>
<tr><td>MOV A,Rn</td><td colspan="2">Move register to accumulator</td><td>0xE8-0xEF</td><td>1</td><td>1</td></tr>
<tr><td>MOV A,direct</td><td colspan="2">Move direct byte to accumulator</td><td>0xE5</td><td>2</td><td>2</td></tr>
<tr><td>MOV A,@Ri</td><td colspan="2">Move indirect RAM to accumulator</td><td>0xE6-0xE7</td><td>1</td><td>2</td></tr>
<tr><td>MOV A,#data</td><td colspan="2">Move immediate data to accumulator</td><td>0x74</td><td>2</td><td>2</td></tr>
<tr><td>MOV Rn,A</td><td colspan="2">Move accumulator to register</td><td>0xF8-0xFF</td><td>1</td><td>1</td></tr>
<tr><td>MOV Rn,direct</td><td colspan="2">Move direct byte to register</td><td>0xA8-0xAF</td><td>2</td><td>3</td></tr>
<tr><td>MOV Rn,#data</td><td colspan="2">Move immediate data to register</td><td>0x78-0x7F</td><td>2</td><td>2</td></tr>
<tr><td>MOV direct,A</td><td colspan="2">Move accumulator to direct byte</td><td>0xF5</td><td>2</td><td>2</td></tr>
<tr><td>MOV direct,Rn</td><td colspan="2">Move register to direct byte</td><td>0x88-0x8F</td><td>2</td><td>2</td></tr>
<tr><td>MOV direct1,direct2</td><td colspan="2">Move direct byte to direct byte</td><td>0x85</td><td>3</td><td>3</td></tr>
<tr><td>MOV direct,@Ri</td><td colspan="2">Move indirect RAM to direct byte</td><td>0x86-0x87</td><td>2</td><td>3</td></tr>
<tr><td>MOV direct,#data</td><td colspan="2">Move immediate data to direct byte</td><td>0x75</td><td>3</td><td>3</td></tr>
<tr><td>MOV @Ri,A</td><td colspan="2">Move accumulator to indirect RAM</td><td>0xF6-0xF7</td><td>1</td><td>2</td></tr>
<tr><td>MOV @Ri,direct</td><td colspan="2">Move direct byte to indirect RAM</td><td>0xA6-0xA7</td><td>2</td><td>3</td></tr>
<tr><td>MOV @Ri,#data</td><td colspan="2">Move immediate data to indirect RAM</td><td>0x76-0x77</td><td>2</td><td>2</td></tr>
<tr><td>MOV DPTR,#data16</td><td colspan="2">Load 16-bit constant into active DPH and DPL in LARGE mode</td><td>0x90</td><td>3</td><td>3</td></tr>
<tr><td>MOVC A,@A+DPTR</td><td colspan="2">Move code byte relative to DPTR to accumulator</td><td>0x93</td><td>1</td><td>5</td></tr>
<tr><td>MOVC A,@A+PC</td><td colspan="2">Move code byte relative to PC to accumulator</td><td>0x83</td><td>1</td><td>4</td></tr>
<tr><td rowspan="2">MOVX A,@Ri</td><td rowspan="2">Move external RAM (8-bit address) to A</td><td>XDM</td><td rowspan="2">0xE2-0xE3</td><td rowspan="2">1</td><td>3*</td></tr>
<tr><td>SXDM</td><td>3</td></tr>
<tr><td rowspan="2">MOVX A,@DPTR</td><td rowspan="2">Move external RAM (16-bit address) to A</td><td>XDM</td><td rowspan="2">0xE0</td><td rowspan="2">1</td><td>2*</td></tr>
<tr><td>SXDM</td><td>2</td></tr>
<tr><td rowspan="3">MOVX @Ri,A</td><td rowspan="2">Move A to external XDM (8-bit address)</td><td>ODE inside ROM/RAM</td><td rowspan="3">0xF2-0xF3</td><td rowspan="3">1</td><td>4*</td></tr>
<tr><td>Other cases</td><td>5*</td></tr>
<tr><td>Move A to external SXDM (8-bit address)</td><td>All cases</td><td>3</td></tr>
<tr><td rowspan="3">MOVX @DPTR,A</td><td rowspan="2">Move A to external XDM (16-bit address)</td><td>CODE inside ROM/RAM</td><td rowspan="3">0xF0</td><td rowspan="3">1</td><td>3*</td></tr>
<tr><td>Other cases</td><td>4*</td></tr>
<tr><td>Move A to external SXDM (16-bit address)</td><td>All cases</td><td>2</td></tr>
<tr><td>PUSH direct</td><td colspan="2">Push direct byte onto IDM stack</td><td>0xC0</td><td>2</td><td>3</td></tr>
<tr><td>POP direct</td><td colspan="2">Pop direct byte from IDM stack</td><td>0xD0</td><td>2</td><td>2</td></tr>
<tr><td>XCH A,Rn</td><td colspan="2">Exchange register with accumulator</td><td>0xC8-0xCF</td><td>1</td><td>2</td></tr>
<tr><td>XCH A,direct</td><td colspan="2">Exchange direct byte with accumulator</td><td>0xC5</td><td>2</td><td>3</td></tr>
<tr><td>XCH A,@Ri</td><td colspan="2">Exchange indirect RAM with accumulator</td><td>0xC6-0xC7</td><td>1</td><td>3</td></tr>
<tr><td>XCHD A,@Ri</td><td colspan="2">Exchange low-order nibble indirect RAM with A</td><td>0xD6-0xD7</td><td>1</td><td>3</td></tr>
</table>

5.16.5. Program Branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	4
LCALL addr16	Long subroutine call	0x12	3	4
RET	Return from subroutine	0x22	1	4
RETI	Return from interrupt	0x32	1	4
AJMP addr11	Absolute jump	0x01-0xE1	2	3
LJMP addr16	Long jump	0x02	3	4
SJMP rel	Short jump (relative address)	0x80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JZ rel	Jump if accumulator is zero	0x60	2	4
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JC rel	Jump if carry flag is set	0x40	2	3
JNC	Jump if carry flag is not set	0x50	2	3
JB bit,rel	Jump if direct bit is set	0x20	3	5
JNB bit,rel	Jump if direct bit is not set	0x30	3	5
JBC bit,direct rel	Jump if direct bit is set and clear bit	0x10	3	5
CJNE A,direct rel	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE A,#data rel	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE Rn,#data rel	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CJNE @Ri,#data rel	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
NOP	No operation	0x00	1	1

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

	Rating	Units
VDD, VDD_ADC, VDD_OP, ADC_VREF	-0.3 ~ 6	V
P00~P07, P10~P17, P20~P27, P30~P34 , RESET, ADC_IN	-0.3 ~ 6	V
Operating Temperature (T_A)	-40 to +85	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
IOSC Frequency	F_{OSC}	8.0×(1-2%)	8.0	8.0×(1+2%)	MHz	±2% at 2.4V~5.5V
PLL Frequency	F_{PLL}	F_{PLL}×(1-2%)	F_{PLL}	F_{PLL}×(1+2%)	MHz	±2% at 2.4V~5.5V

6.3. DC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	
Operating Current	I_{OP}	-	15.0	-	mA	SYSCLK= 65.3824MHz @ 5.0V,no load
Standby Current	I_{STBY}	-	10	18	uA	VDD = 5.5V LVR Disable
Input High Level	V_{IH}	0.7*VDD	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.3*VDD	V	VDD = 5.0V
Output High Level	V_{OH}	0.8*VDD	-	-	V	I_{OH} = -15mA at VDD = 5.0V , PX_DRV = 0,
Output Low Level	V_{OL}	-	-	0.2*VDD	V	I_{OL} = 15mA at VDD = 5.0V PX_DRV = 0,
Output High Current	I_{OH_DRV}	-	15	-	mA	V_{OH}=VDD(5V)*0.8 PX_DRV = 0
	I_{OH}	-	8	-	mA	V_{OH}=VDD(5V)*0.8 PX_DRV = 1
Output Low Current	I_{OL_DRV}	-	15	-	mA	V_{OL}=VDD(5V)*0.2 PX_DRV = 0
	I_{OL}	-	8	-	mA	V_{OL}=VDD(5V)*0.2 PX_DRV = 1
Input Pull High Resistor	R_{PH1}	30	50	70	KΩ	VDD = 5.0V
Input Pull Low Resistor	R_{PL1}	30	50	70	KΩ	VDD = 5.0V
Low Voltage Reset 1	V_{LVR1}	2.4×(1-5%)	2.4	2.4×(1+5%)	V	SYS_CTRL3[2:1]=00
Low Voltage Reset 2	V_{LVR2}	2.8×(1-5%)	2.8	2.8×(1+5%)	V	SYS_CTRL3[2:1]=01
Low Voltage Reset 3	V_{LVR3}	3.2×(1-5%)	3.2	3.2×(1+5%)	V	SYS_CTRL3[2:1]=10
Low Voltage Reset 4	V_{LVR4}	4.2×(1-5%)	4.2	4.2×(1+5%)	V	SYS_CTRL3[2:1]=11

6.4. ADC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_ADC	V_{LVR}	5.0	5.5	V	SYS_CTRL3[0]=1'b1
ADC Channel Input Voltage Range	V_{ADCIN}	0	-	ADC_VREF	V	
ADC Clock Period	T_{AD}	-	61.17	-	ns	Depended on system clock
Input Channel		-	-	13	channel	
Resolution		12			Bit	VDD_ADC=5V
No Missing Code		10			bits	VDD_ADC=5V
ADC Conversion Time	T_{CON}	-	1.04	-	us	ADCLK = SYSCLK(65.3824M)/4 ADC_CTRL2[2:0] = 3'b011
Integral Linearity Error	E_{INL}	-	±2	±3	LSB	VDD_ADC=5V
Differential Linearity Error	E_{DNL}	-	-1~+2	-1~+3	LSB	VDD_ADC=5V

6.5. OP and Comparator Characteristics (T_A = 25℃)

6.5.1. OP

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.7	-	5.5	V	
OP1 Input Offset	V_{inos}	-4	0	+4	mV	VDD = 4.0~5.5V
OP0/2 Input Offset	V_{inos}	-	30	-	mV	VDD = 4.0~5.5V
OP0~2 input Range	V_{in}	0	-	VDD-1	V	
Setting Time	Ts	-	-	30	us	Input to output @VDD=4V Load = 50pF

6.5.2. Comparator

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.7	-	5.5	V	
Comparator Input Range	V_{in}	0	-	VDD	V	VDD=5.0V

7.PACKAGE INFORMATION

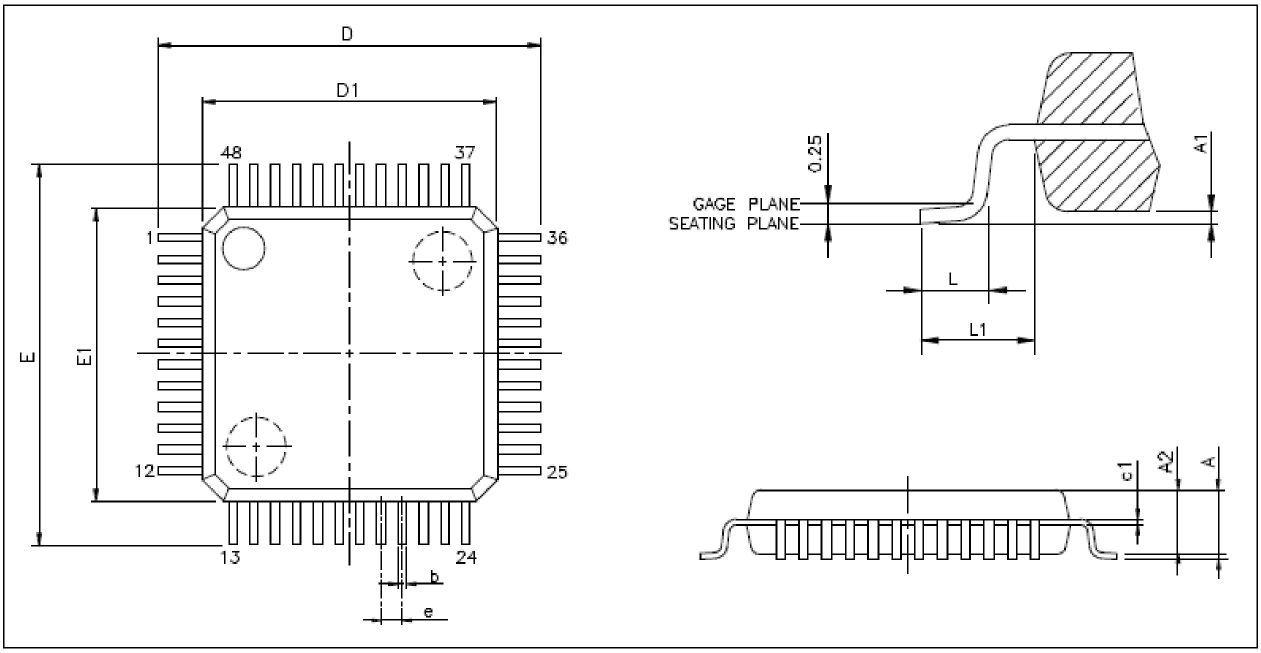
7.1. Ordering Information

Product Number	Package Type
GPM8F3331B-QL231	LQFP48
GPM8F3331B-QV041	QFN32

Note1: Package form number (x = 1 - 9, serial number).

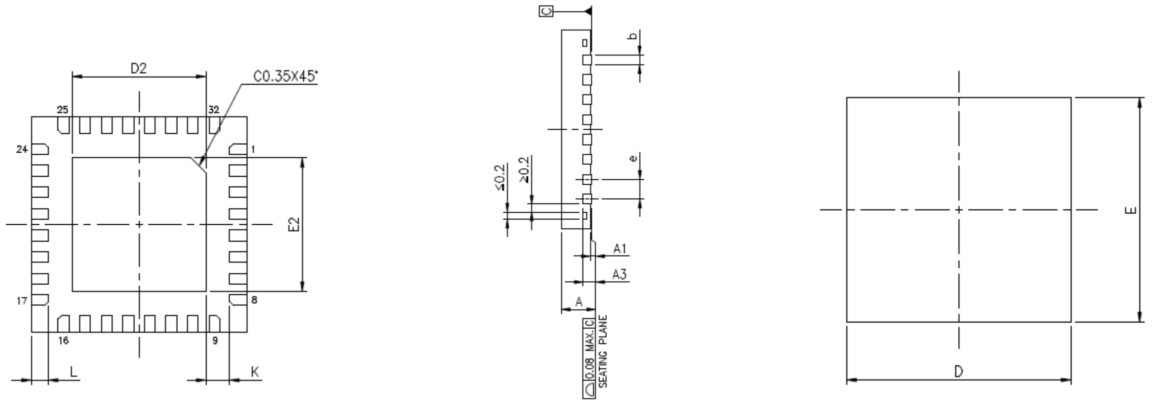
7.2. Package Information

7.2.1. LQFP48



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
C1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
b	0.17	-	0.27
L	0.45	-	0.75
L1	1.00 REF		

7.2.2. QFN32



Symbol	Millimeter		
	Min.	**Nom.**	**Max.**
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.18	0.25	0.30
D		5.00BSC	
E		5.00BSC	
e		0.50BSC	
L	0.35	0.40	0.45
K	0.20	--	--
D2	3.15	3.20	3.25
E2	3.15	3.20	3.25

Note:

1. All dimensions are in millimeters.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

8.DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
Aug. 24, 2021	0.3	Modify the maximum standby current of DC characteristics.	165
Jun. 19, 2020	0.2	Modify absolute maximum ratings table	166
Jan. 20, 2020	0.1	Preliminary Version.	171