# ESP32

## Audio Design Guidelines

Version 1.0

Espressif Systems

# About This Guide

The guidelines outline recommended design practices when developing Audio products based on the ESP32.

## Release Notes

| Date | Version | Release notes |
|---|---|---|
| 2019.01 | V1.0 | Initial release. |

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# 1. Schematic Design

The circuit design of an audio product, based on the ESP module provided by Espressif, can be broken down into three major sections:

- Power supply and GND plane.
- Design rules of audio chips.
- Pin configuration of the ESP32 module.

## 1.1. Power Supply and GND Plane

### 1.1.1. USB/Battery Power Scheme

When the module works in Wi-Fi mode, peak current in the circuit is very high. The suggested output current for the module's power supply is no less than 500 mA. As audio boards generally require an external battery, your design may need a charging management chip, for example AP5056, to charge the battery. You can choose a chip according to your actual needs.

If the battery is used to power the whole system, please make sure that it is connected to the circuit and that the VBAT pin of the charging management chip, serving as the input of the system power supply, is connected to the positive terminal of the battery. As soon as the charging management chip detects the battery, it starts supplying current of the nominal value identified in its specification, but if the battery is not detected, the output current is very small, and power supply for the circuit may be insufficient.

You can avoid this problem by adding a USB/Battery power supply switch circuit into the design (as shown in Figure 1-1). For example, if a USB cable is plugged in, VBAT pin is cut off from the system and the power is supplied over USB; otherwise, the power will be supplied over VBAT.

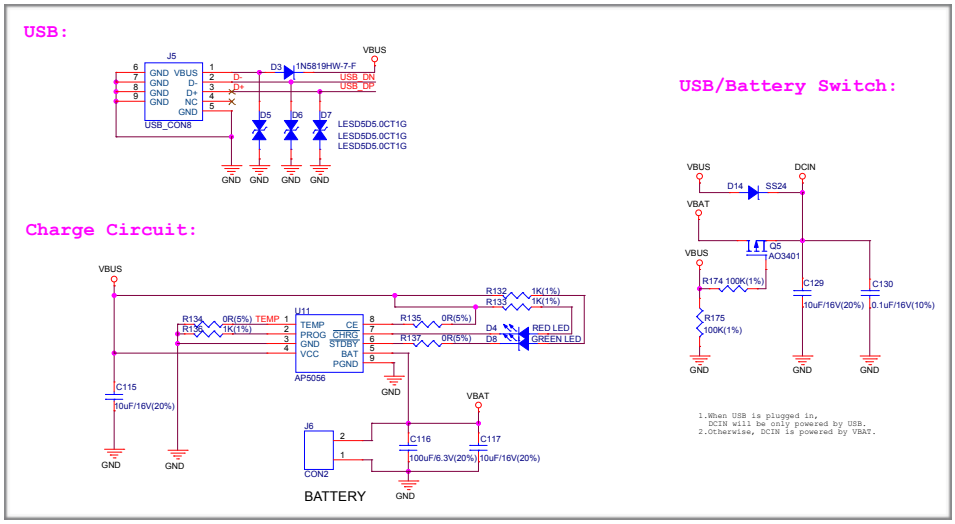


**Figure 1-1. USB/Battery Power Supply Circuit**

### 1.1.2. Power Scheme for Peripherals

Peripherals that require power supply on an audio board include Wi-Fi module, Codec module, DSP module, PA power amplifier module, Micro SD card module, LED module, etc. While PA power amplifier is directly powered by USB/Battery, the other modules are powered through the power management chip, which converts the USB/Battery voltage to the voltage they require.

For increased reliability, you can reserve a separate power management chip and optional resistors for each module in case an independent (backup) power supply is needed. During debugging, you can determine whether some chips can be removed, based on the actual test results. The power management chip of your choice should meet the circuit requirements for input and output of current and voltage, low noise, efficiency and other aspects of the circuit. For example:

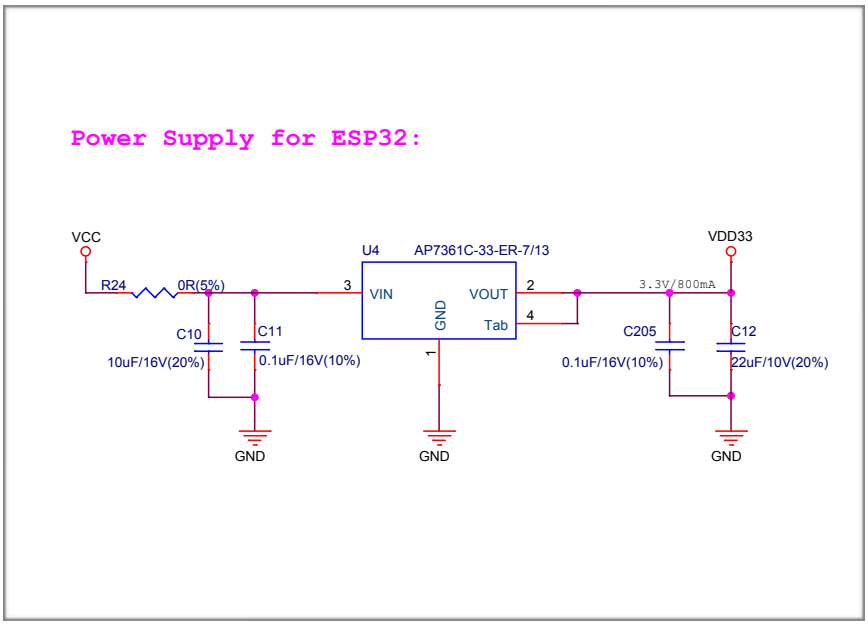


**Figure 1-2. Power Supply Management Circuit for Peripherals**

### 1.1.3. Ground Plane Splitting Scheme

For the above-listed modules (Wi-Fi module, Codec module, DSP module, PA power amplifier module, Micro SD card module, LED module, etc.), their reference ground planes should be separated according to the actual situation. For example, the reference ground plane of Wi-Fi module and Micro SD card is DGND; the reference ground plane for PA power amplifier and external loudspeaker is AGND; Codec module, DSP module, LED light and other chips also have their own reference ground planes. It is also recommended to provide a separate ground plane for the input power module. These planes should be connected by a short circuit with a 0R resistor (Packaging should be above 0603), such as at the following figure:

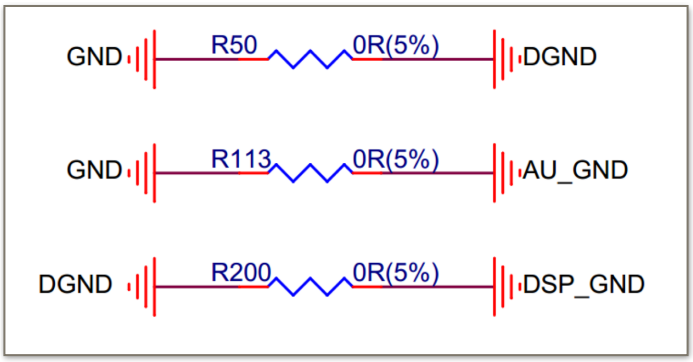


Figure 1-3. Circuit for Splitting Ground Planes

## 1.2. Design Rules for Audio Chip

Each chip has its own design rules. For example, a codec might require very strict rules for digital and analog signals, otherwise unwanted noise might occur. Digital signal processors (DSP) might require different reference ground planes. Some PA power amplifiers can support differential inputs, while others support only single-ended input, etc.

> 📖 ***Note:***
>
> *In your design, you need to refer to the datasheet or reference design of the chips provided by the original manufacturer.*

For example:

The specific design rules for a DSP:

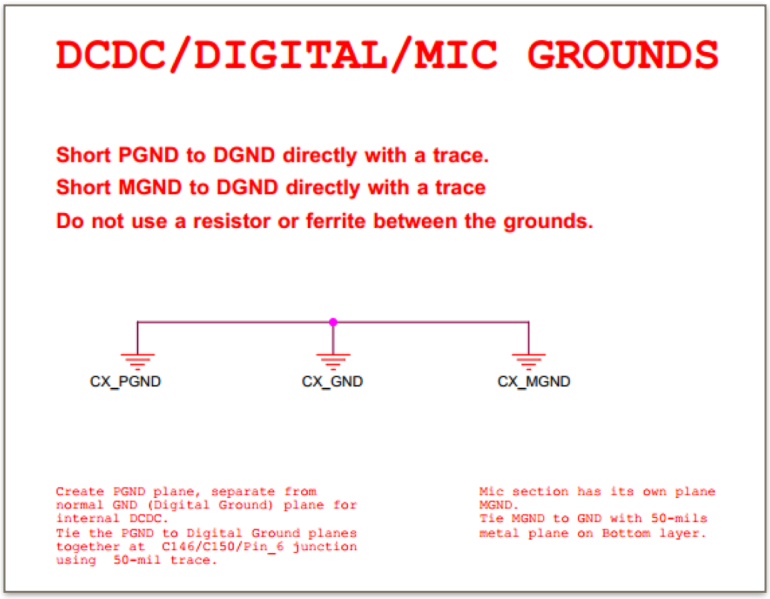


Figure 1-4. Reference Circuit Design for a DSP Ground Plane

The separation of AGND and DGND for a Codec:

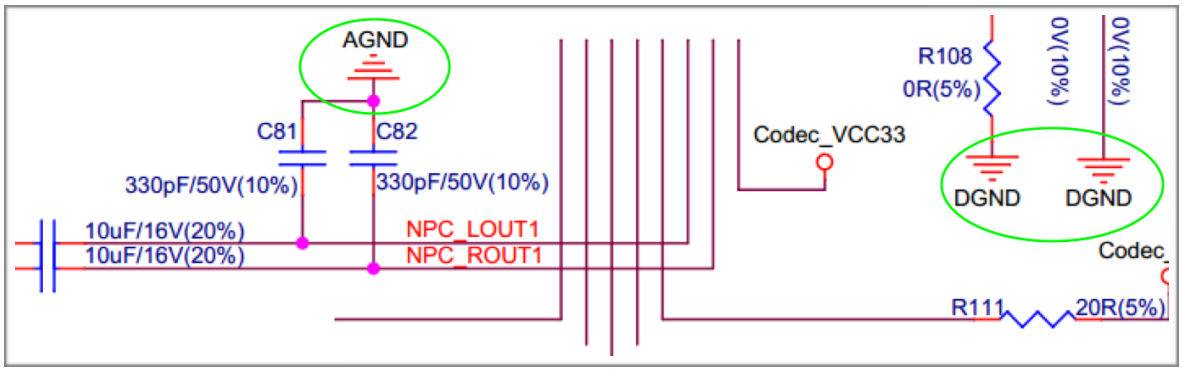


Figure 1-5. Reference Circuit Design for a Codec Ground Plane

## 1.3. Pin Configuration of ESP32

Most pins of an ESP32 module can be reconfigured with high flexibility, according to your requirements, but there are still some guidelines that you need to follow.

### 1.3.1. Module Power Supply

At the 3.3 V power supply input pin, it is recommended to add a 100 uF large capacitor with an extra filter capacitor of 0.1 uF close to the module power supply pin.

### 1.3.2. Module Enable

A 10 K pull-up resistor and a 1 uF ground capacitor are highly recommended on CHIP_EN pin to form an RC delay circuit to avoid level instability on CHIP_EN end in power-on process. In addition, CHIP_EN serves as the reset pin, so it is recommended to connect it to a button for the reset operation.

### 1.3.3. Input-only Pins

Some pins of ESP32 can be used for input only, such as CHIP_EN, SENSOR_VP, SENSOR_CAPP, SENSOR_CAPN, SENSOR_VN, IO34, IO35, etc.

> 📖 ***Note:***
>
> - *SENSOR_VP, SENSOR_CAPP, SENSOR_CAPN and SENSOR_VN are recommended for use as ADC detection. The recommended voltage detection range is 0 V~ 2.5 V. Also, adding a 0.1 uF capacitor to the pin close to ESP32 is suggested.*
> - *In ESP32 series modules, SENSOR_CAPP and SENSOR_CAPN pins are not led out, so only SENSOR_VP and SENSOR_VN can be used.*

For example:

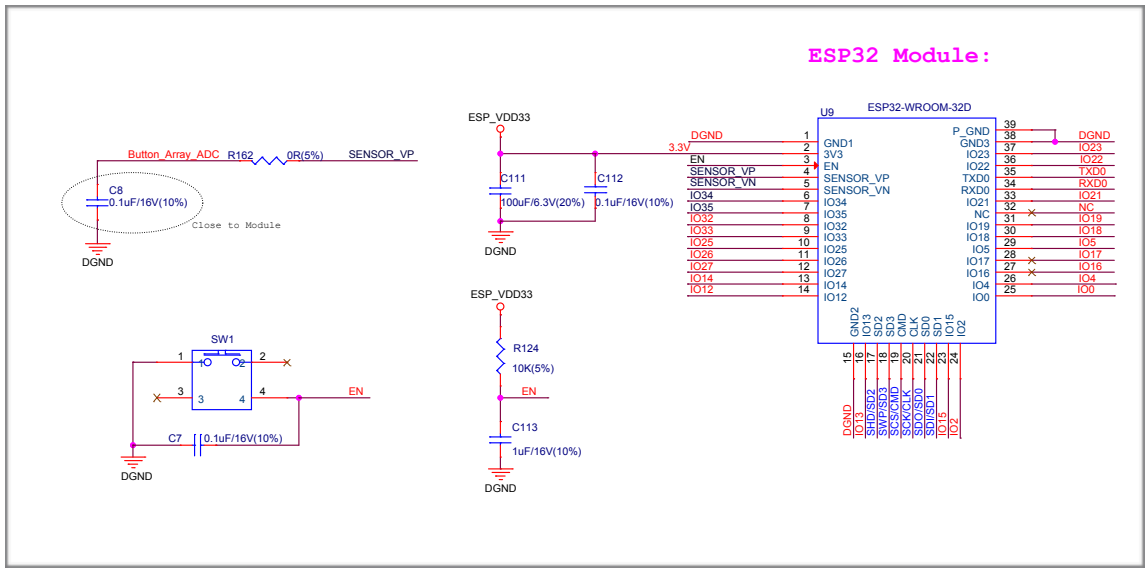


**Figure 1-6. Reference Circuit for Part of ESP32 Pin Configuration**

### 1.3.4. Dedicated Pins

- SHD/SD2, SWP/SD3, SCS/CMD, SCK/CLK, SDO/SD0, and SDI/SD1 used for connecting SPI Flash integrated within the module are not recommended for other functions.
- If ESP32-WROVER series modules are selected, GPIO16 is reserved as the chip selection pin and GPIO17 as clock of PSRAM within the module, so these two GPIOs are not recommended for other functions.
- TXD0/RXD0 are UART0 pins used for flashing and communication; they are not recommended for other functions.

> 📖 ***Note:***
>
> *ESP32 cannot identify USB directly, so a USB to UART chip is needed in your design, such as CP2102-GM. The UART pin of the chip is connected with the UART0 pin of ESP32, which can be used to flash programs to ESP32 and serves as an interactive interface with the PC. In your design, it is recommended to reserve test points for TXD0 and RXD0.*

For example:

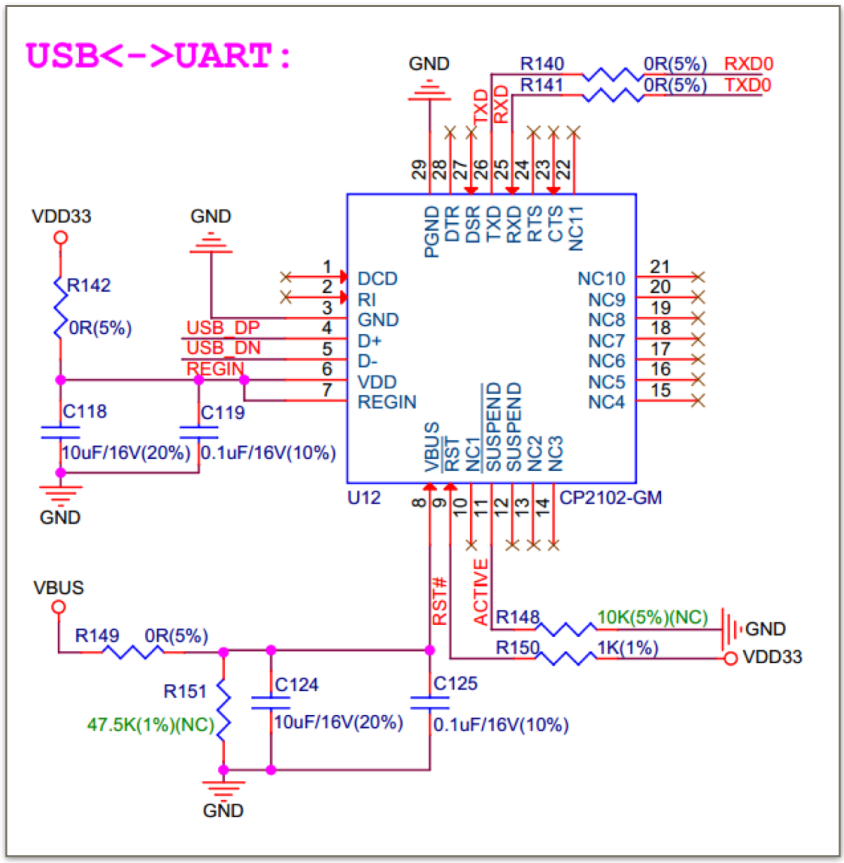


Figure 1-7. Reference Circuit for USB-UART Chip

### 1.3.5. Strapping Pins and Other Special Pins

- GPIO0 is one of the strapping pins, and its level state in the power-on reset process is related to download:
  - "1": enter Flash startup mode, and the chip defaults to "1".
  - "0": enter download mode.

Meanwhile, GPIO0 can also connect to other chips, such as MCLK (master clock), so using GPIO0 for other functions is not recommended.

- GPIO2 is another strapping pin, and its level state in the power-on reset process is also related to download:
  - "0": enter download mode, and the chip defaults to "0".

Meanwhile, GPIO2 can be used for connection to SDIO/MMC (for example, SD card), so using GPIO2 for other purposes is not recommended.

> 📖 ***Note:***
>
> *In your design, it is recommended to reserve test points for GPIO0 and GPIO2, or to connect a button for downloading.*

For example:

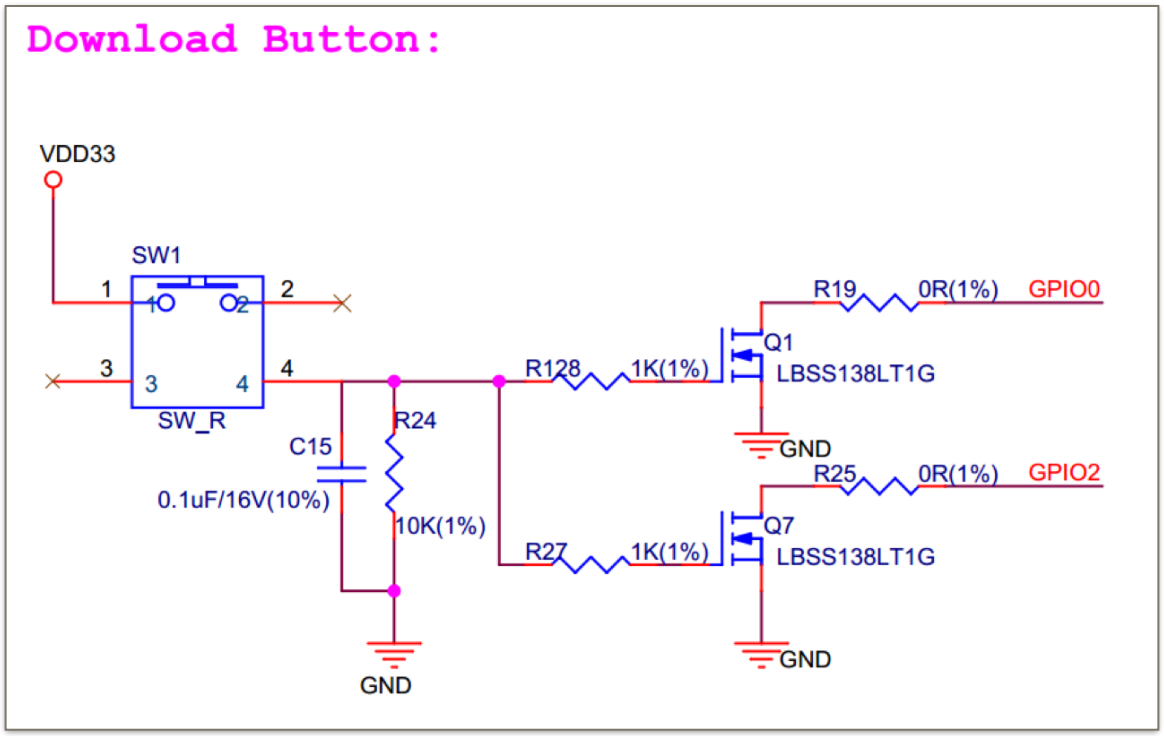


**Figure 1-8. Reference Circuit for Download Button**

- GPIO12 is yet another strapping pin, and its level state in the power-on reset process is related to the output voltage of the LDO inside the chip:
  - "0": output 3.3 V, and the chip defaults to "0";
  - "1": output 1.8 V.

> 📖 ***Note:***
>
> *The above-mentioned voltages are related to the power supply voltage of integrated flash and PSRAM in the module.*

Meanwhile, GPIO12 can also serve as the pin to connect SDIO/MMC, such as an SD card, as well as the pin to connect JTAG. Therefore, it is not recommended to use GPIO12 for other purposes. Please pay particular attention to the fact that the level state in the power-on reset process of GPIO12 cannot conflict with the output voltage of LDO.

- Pins used as ADC, DAC, TouchPad, SD card, JTAG, RTC domain pins required in low-power sleep mode, etc. are all special pins. Please refer to *ESP32 Datasheet* while configuring these pins.

# 2. PCB Layout Design

During Audio PCB Layout design, pay attention to the following sections:

- General principles of PCB Layout
- Key points of PCB Layout design
- Power traces, ground traces, and signal traces

## 2.1. General Principles of PCB Layout

### 2.1.1. PCB Layers

A four-layer PCB design is recommended.

- **First layer**: TOP layer for ESP32 module and most of other chips
- **Second layer**: GND layer with a complete GND plane
- **Third layer**: POWER layer to route power traces and part of signal traces
- **Fourth layer**: BOTTOM layer, on which some components are placed, and also power traces and signal traces are routed.

> 📖 ***Note:***
>
> *Components can be placed either on the TOP layer or BOTTOM layer according to the actual situation, but it is recommended to set the adjacent layer of ESP32 module as GND layer. Even if ESP32 module is placed on the BOTTOM layer, it is recommended to set the third layer as a GND layer and the second layer as a POWER layer.*

### 2.1.2. General Guidelines for Routing Traces

General guidelines for routing traces are as follows:

- Try to plan out the shortest route and pass through the least holes, avoid unnecessary bending and holes.
- Use obtuse angles to keep the layout as clean and tidy as possible, avoid using right angles and acute angles or hiding small line segments among these angles
- Avoid routing traces on the layers under crystal oscillator, large inductance devices and other sensitive devices.

For example:

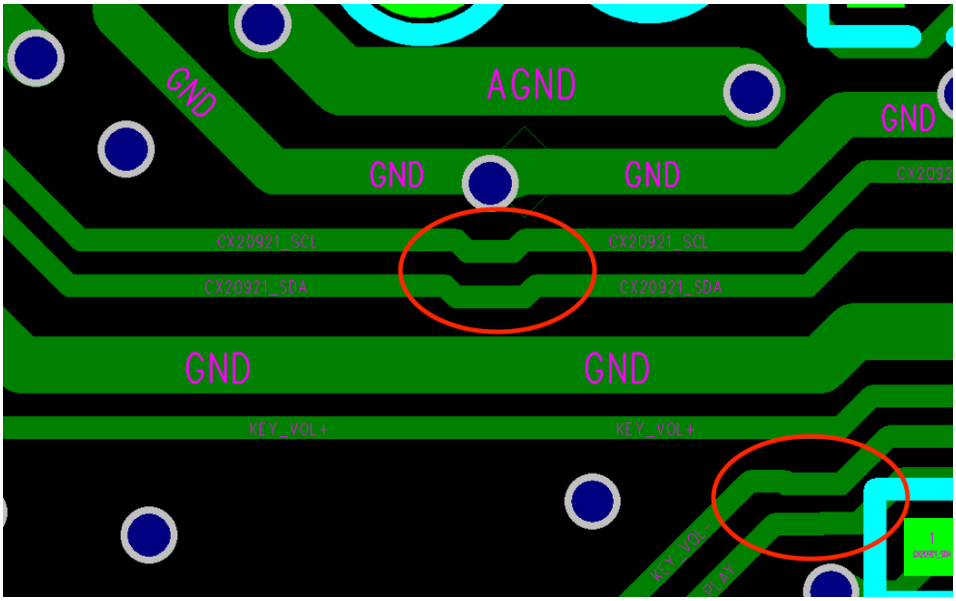


Figure 2-1. Non-recommended Trace Routing

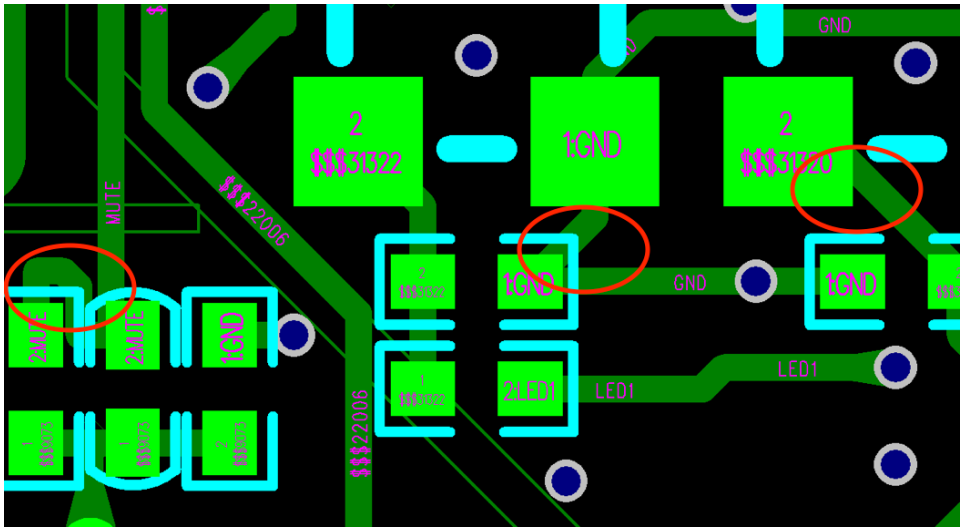


Figure 2-2. Non-recommended Trace Routing

## 2.2. Key Points of PCB Layout Design

### 2.2.1. Positioning an ESP32 Module on a Baseboard

Place the module's PCB antenna area outside the baseboard, but put the module as close to the edge of the baseboard as possible, so that the antenna's feed point is closest to the board edge. For example:

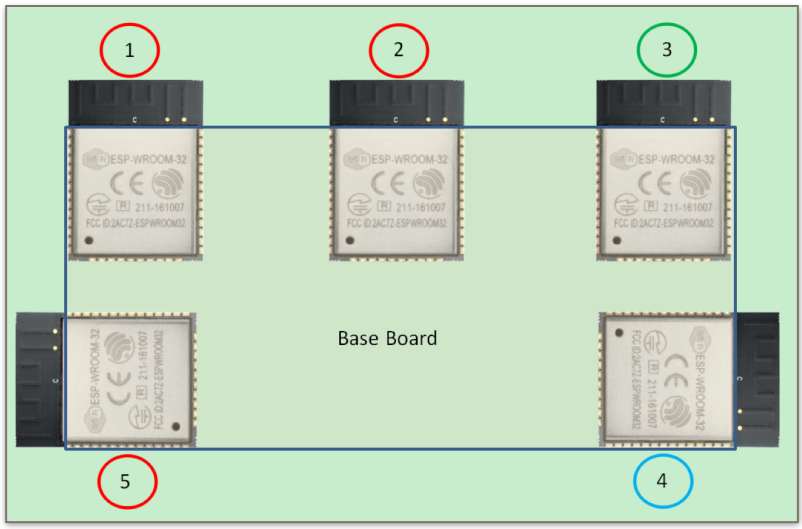


Figure 2-3. ESP32 Module Antenna Position on Baseboard

> 📖 ***Note:***
>
> *As shown in Figure 2-3, the recommended position for an ESP32 module on the baseboard is:*
>
> *Position 3: Highly recommended.*
>
> *Position 4: Recommended.*
>
> *Position 1, 2, 5: Not recommended.*

If the recommended positioning requirements cannot be met, please at least make sure that the module is not covered by any metal shell, and the module's antenna area plus 15 mm outwards is kept clear (no copper, routing, components) as shown in Figure 2-4.

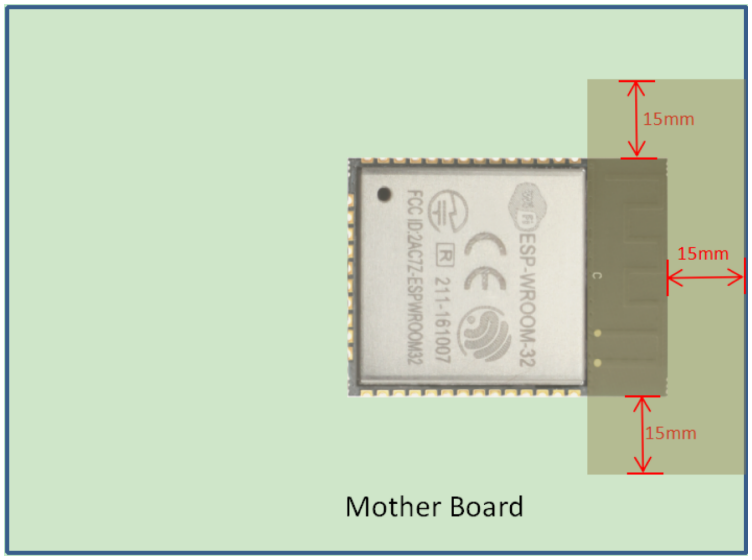


Figure 2-4. Clearance Zone for ESP32 Module's Antenna on the Baseboard

The module's antenna area should be as far away from other parts as possible, especially from the audio output. The antenna area is recommended to be in the opposite direction of the audio output, or at least at 90 degrees if the former cannot be satisfied. For example:

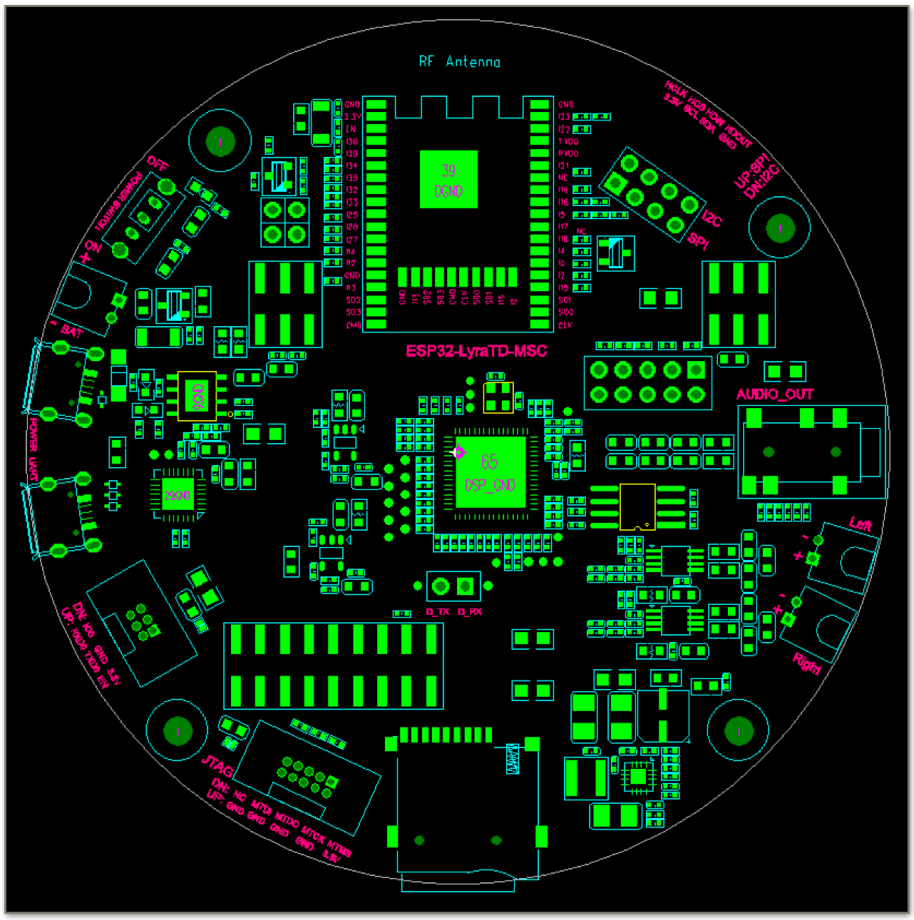


Figure 2-5. Reference Design for Module Placement

### 2.2.2. Positioning Plug-in Components

For the USB interface, battery socket holder, power switch, SD card, headphone socket, external speaker socket, debugging pin header, mounting hole, etc., the positioning of their components should adhere to the following principles:

- Taking component structures into account, trying to make mounting/connecting easy.
- Facilitating the actual debugging operation
- Assisting trace routing

> 📖 ***Note:***
>
> *In particular, you need to pay special attention to plug-in direction, pin sequence, positive and negative polarity of these components. It is recommended to label these points at the Top Overlayer.*

For example:

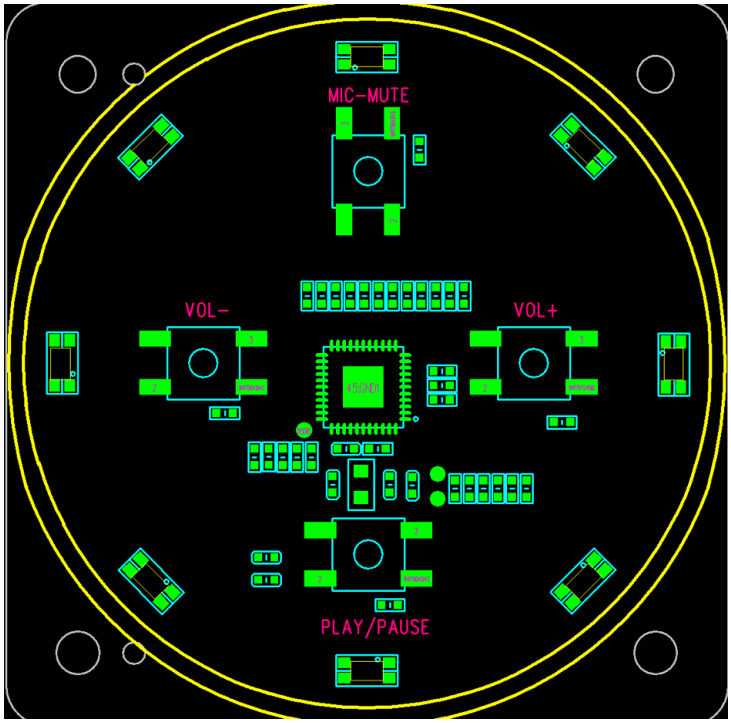


Figure 2-6. Positioning Plug-in Components

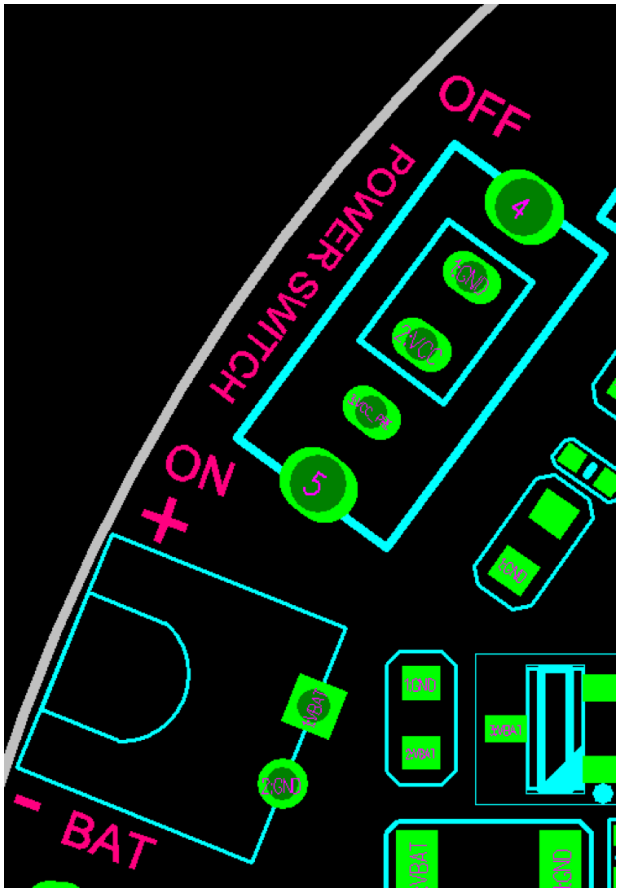


Figure 2-7. Positioning Plug-in Components

### 2.2.3. Positioning Chip Components

It is recommended to place the chip components and their peripherals together, especially the filter capacitor for the power supply. These capacitors must be placed as close to the power pins as possible and distributed evenly. Please make sure you have a filter capacitor near each power pin, but do not stack all the capacitors in one place.

For the sake of routing and ground splitting, modules sharing the same ground plane should be placed near, as well as the functionally related modules (Codec, PA power amplifier and speaker of Audio chip, as well as USB interface, charging module and battery interface). See the picture below.

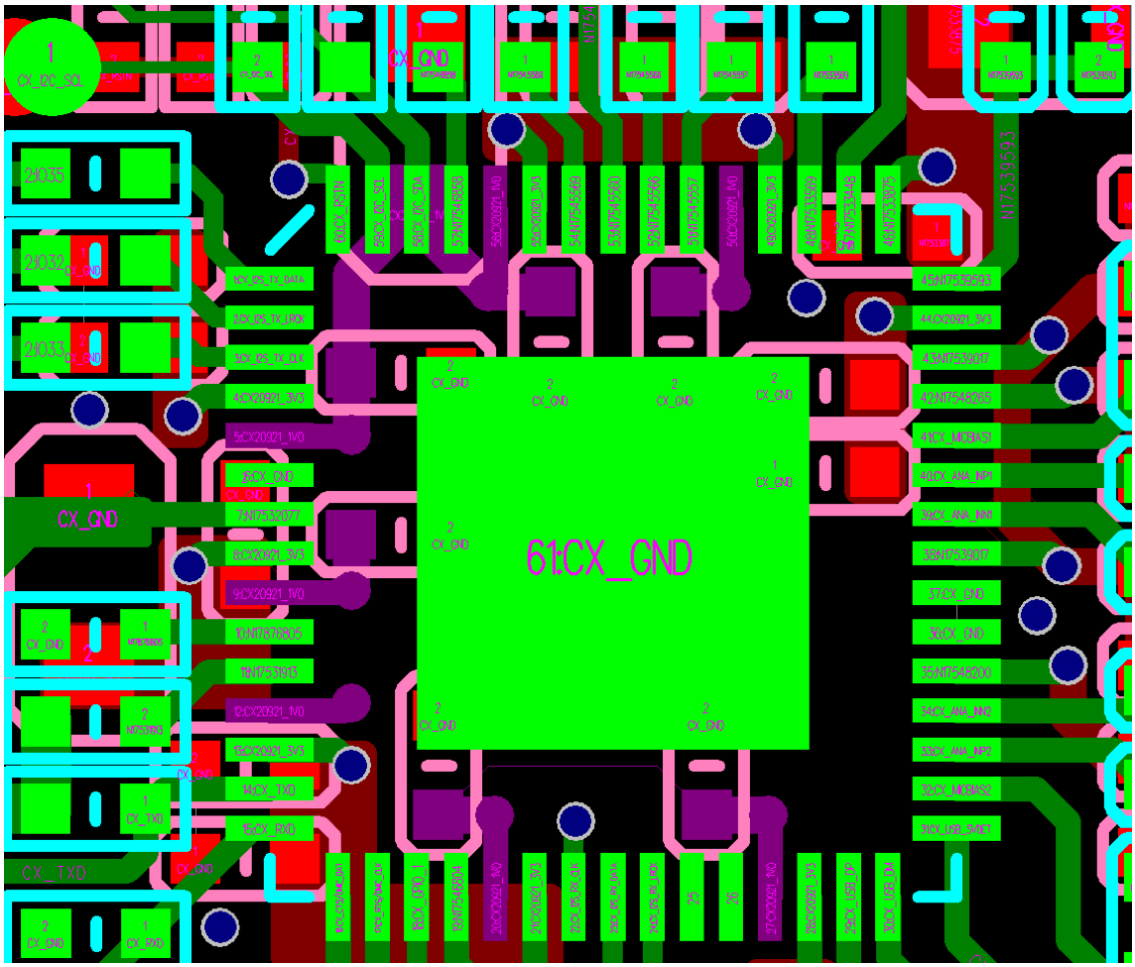


Figure 2-8. Reference Placement for Chip Components

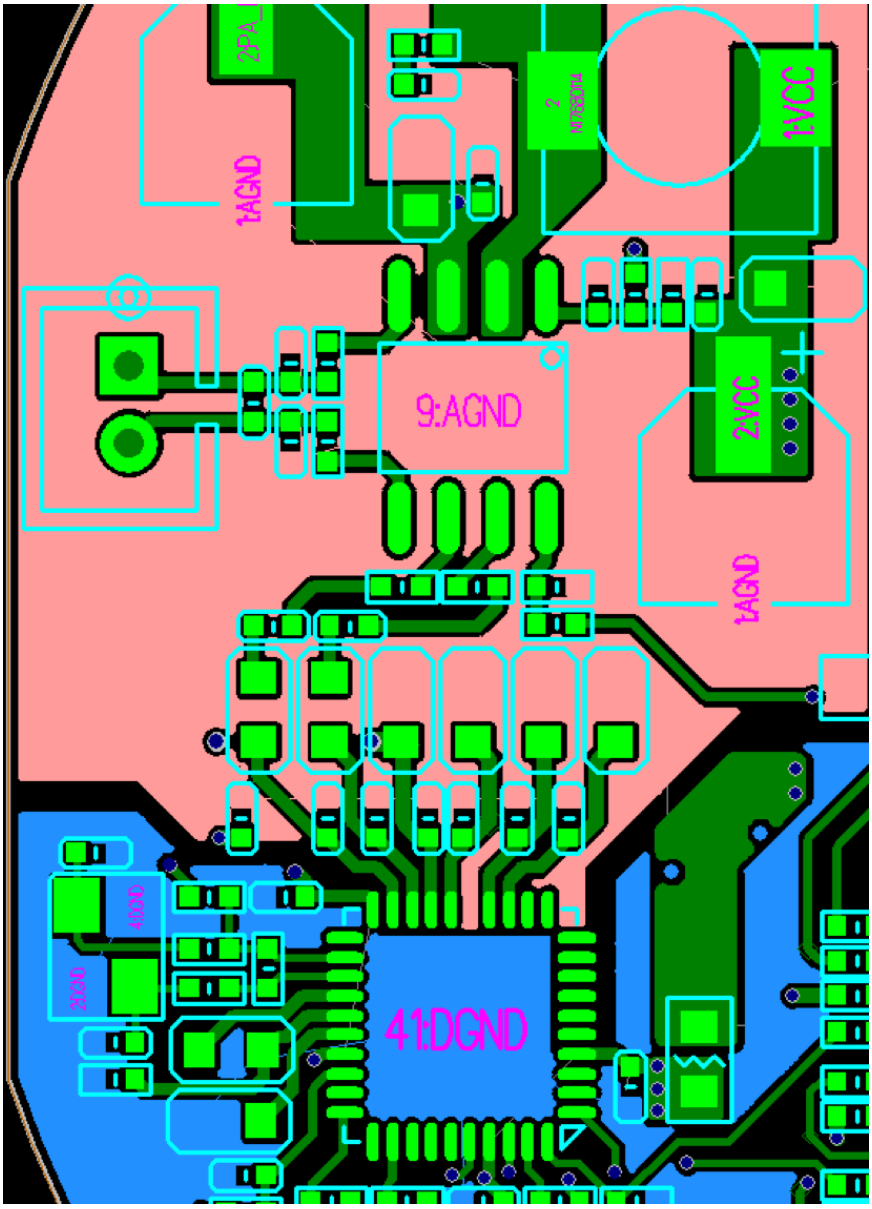


Figure 2-9. Reference Placement for Chip Components

## 2.3. Power Traces, Ground Traces, and Signal Traces

### 2.3.1. Power Traces Routing

The width of power traces and vias (holes) through layers should meet the requirements of current flowing:

- Traces of 1 mm wide should be able to carry the current of up to 1 A.
- A 0.25 mm via on a 0.5 mm pad should be able to carry the current of up to 500 mA.
- If copper foil is laid, please make sure that the width of each power trace is constant along their length, with no bottlenecks due to other traces or vias.

- It is recommended to separate different power traces from each other by ground traces and to plate copper for power supplies on adjacent layers to avoid overlapping. It helps to reduce mutual interference.

In the figure below, red and purple represent power copper for different purposes, and blue represents ground copper.

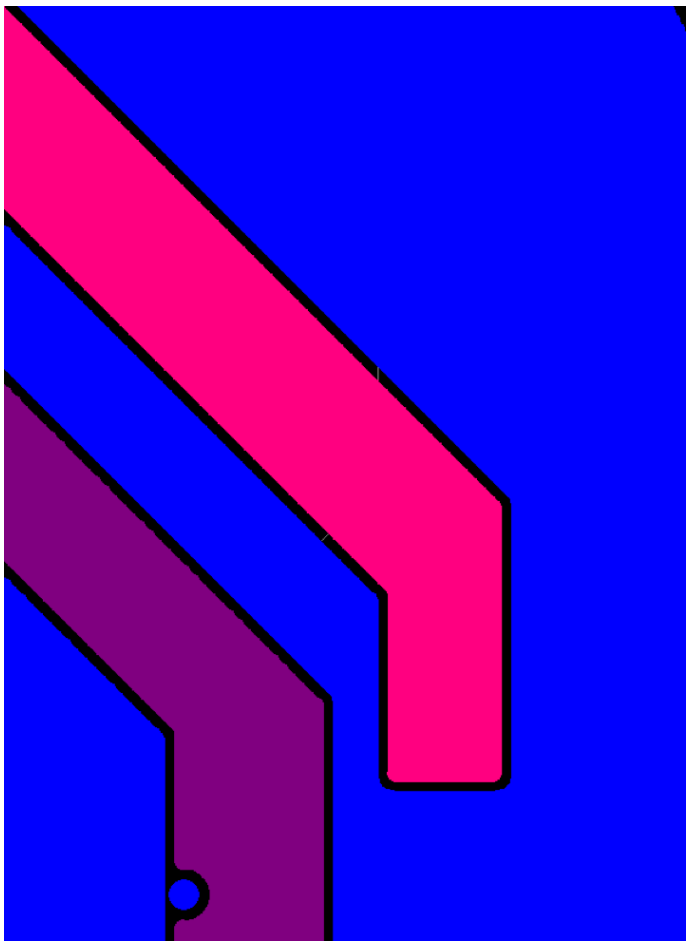

**Figure 2-10. Recommended Power Routing**

### 2.3.2. Ground Traces Routing

Different reference ground planes should be separated. Please keep the cutting lines consistent on all layers and drill more ground holes around the 0R resistors that connect the reference grounds. It is also recommended to drill as many ground holes as possible close to the devices' GND pins, especially in the area of the power supply's filter capacitor.

If there is a thermal pad in the middle of the chip, it is suggested to drill no less than 9 evenly-distributed ground holes.

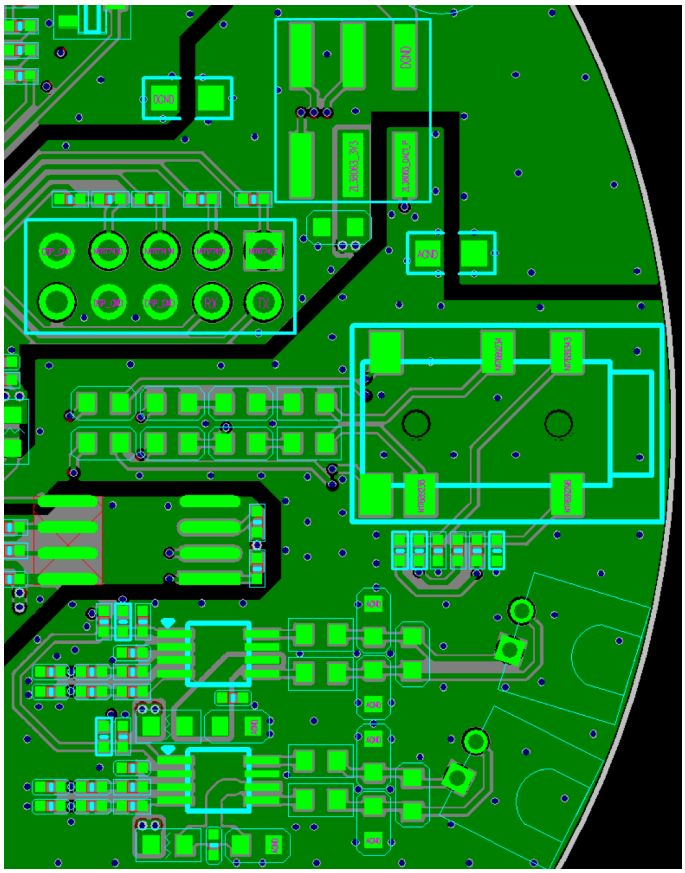

Figure 2-11. Reference Design for Ground Trace Routing

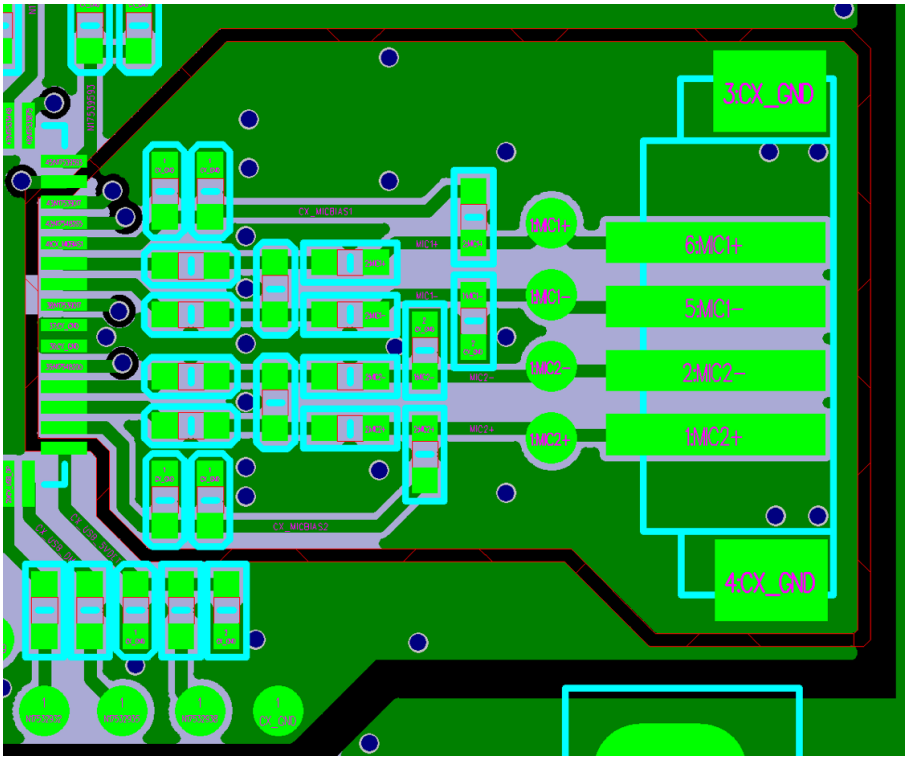


Figure 2-11. Reference Design for Ground Trace Routing

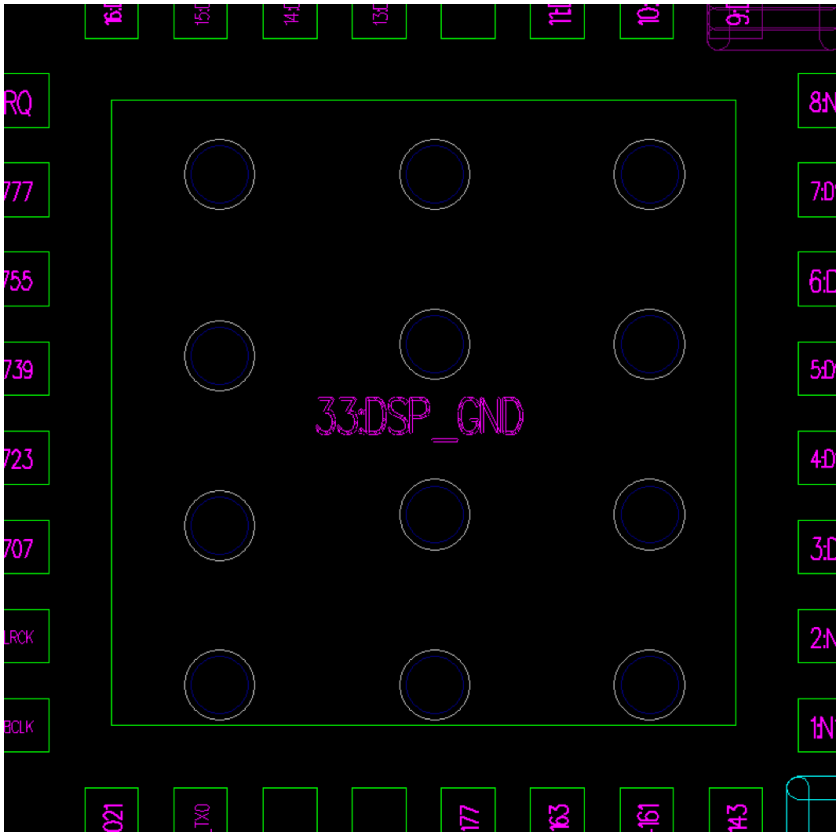


Figure 2-11. Reference Design for Ground Trace Routing

### 2.3.3. Signal Traces Routing

- For the I2C, I2S, and UART groups, each respective group's traces should run parallel with as wide spacing as possible and be isolated from other groups with GND copper foil. If isolation is not possible due to limited space, please at least increase the interval between traces belonging to different groups.
- The signal traces for “Reset” should be as short as possible and isolated from other traces by ground traces or by extending the distance to reduce interference.
- The signal traces for audio input and output need to be enclosed with ground traces and surrounded by more ground holes for shielding.
- TouchPad trace routing must be done in accordance with the *relevant guidelines* to achieve the best performance.

The figures below show some relevant examples (the blue color represents ground copper).


Figure 2-14. Reference Design UART Trace Routing

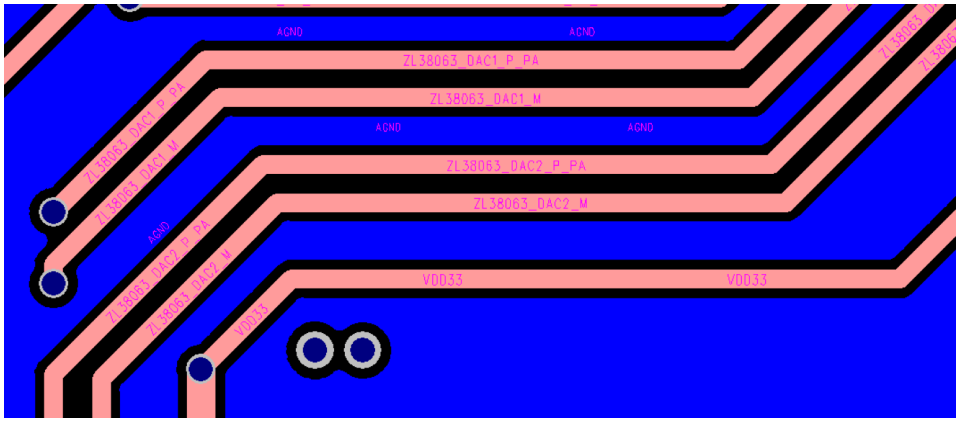


Figure 2-15. Reference Design for Audio Signal Trace Routing

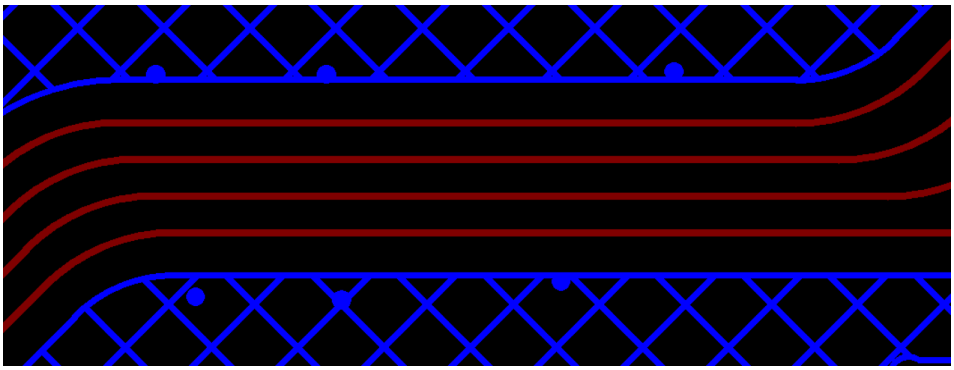

Figure 2-16. Reference Design for TouchPad Traces Routing

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