BL616/BL618

Datasheet

Version: 1.5

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Features

- Wireless (Tier-1 RF Performance)
  - 2.4 GHz RF transceiver
  - Wi-Fi 6 (IEEE 802.11 b/g/n/ax)
  - Bluetooth® 5.3 Dual-mode (BT+BLE)
  - IEEE 802.15.4(Zigbee/Thread)
  - Wi-Fi Fast connection with BLE assistance
  - Wi-Fi/Bluetooth/802.15.4 Coexistence
  - Wi-Fi Security WPS/WEP/WPA/WPA2/WPA3
  - Wi-Fi 20/40MHz BW, 1T1R, up to 229.4 Mbps
  - Support LDPC, STBC, Beamformee, DL/UL OFDMA, MU-MIMO, TWT (Target Wake Time), SR(Spatial Reuse), DCM (Dual Carrier Modulation), ER (Extended Range)
  - Support Aggregation (AMPDU, AMSDU), Immediate Block Ack, Fragmentation and Defragmentation
  - Support RX diversity
  - Support IEEE 802.11e QoS WMM (Wi-Fi MultiMedia), IEEE 802.11w PMF (Protected Management Frames)
  - STA, SoftAP, STA+SoftAP and sniffer modes
  - Multi-Cloud connectivity
  - Integrated RF balun, PA/LNA
  - Support External PA/LNA
- Microcontroller Subsystem
  - 32-bit RISC-V CPU with FPU and DSP
  - L1 cache
  - RTC timer up to One year
  - Two 32-bit general purpose timers
  - Four DMA channels
  - Dynamic Frequency from 1MHz to 320MHz
  - JTAG development support
  - XIP QSPI flash support
- Audio Codec
  - ADC*1 (MIC, SNR>92dB)
  - DAC*1 (Speaker, SNR>95dB)
  - Support 8/12/16/22.05/24/32/44.1/48KHz
- Memory
  - 532KB SRAM[1]
  - 128KB ROM
  - 4Kb eFuse
  - Embedded 2/4/8MB Flash (Optional)
  - Embedded 4/8MB pSRAM (Optional)
- Video/Image
  - Camera Sensor DVP interface
  - Video Codec MJPEG encoding
  - LCD Display (QSPI, DBI, RGB)
- Security
  - Secure boot; Secure debug
  - XIP QSPI On-The-Fly AES Decryption (OTFAD)
  - Support sensitive SW isolation (TrustZone)
  - AES-CBC/CCM/GCM/XTS modes
  - MD5, SHA-1/224/256/384/512
  - TRNG (True Random Number Generator)

[1] 532K SRAM includes 4K HBN RAM ,16K Dcache RAM and 32K Icache RAM.

  - PKA (Public Key Accelerator) for RSA/ECC
- Peripherals
  - USB 2.0 HS OTG (High-Speed 480MHz)
  - SDIO 2.0 slave
  - SD-card interface
  - Two UART (Support 5V IO)
  - Two I2C, support host mode
  - SPI master/slave
  - I2S master/slave
  - 1 PWM (4 channels with complementary outputs)
  - General-Purpose 12~16-bit ADC
  - General-Purpose 12-bit DAC
  - General analog comparators (ACOMP)
  - Flexible 19 (BL616) or 35 (BL618) GPIOs
- Power Modes (Ultra-low Power modes)
  - Off ; Hibernate (<1uA)
  - Power Down Sleep (flexible)
- Clock
  - Support XTAL 24/26/32/38.4/40MHz
  - Support XTAL 32.768KHz
  - Internal RC 32KHz & 32MHz oscillator
  - Internal System & Audio PLL
- Package Type
  - 40 pin QFN (BL616)
  - 56 pin QFN (BL618)

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1 Overview

BL616/BL618 is Wi-Fi 6 + Bluetooth 5.3 + 802.15.4(Zigbee/Thread) combo chipset for ultra-low-power applications.

BL616/BL618 mainly includes two subsystems, wireless and microcontroller.

Wireless subsystem contains 2.4G radio, Wi-Fi 802.11b/g/n/ax, BT/BLE, and 802.15.4 baseband/MAC designs.

Microcontroller subsystem contains a low-power 32-bit RISC-V CPU with floating point units, DSP units, highspeed cache and memories. Power Management Unit controls low-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include USB2.0, SDIO, Ethernet, SD/MMC, SPI, UART, I2C, I2S, PWM, GPDAC, GPADC, Audio, ACOMP and GPIOs. Flexible GPIO configurations are supported. BL616 has total 19 GPIOs and BL618 has total 35 GPIOs.

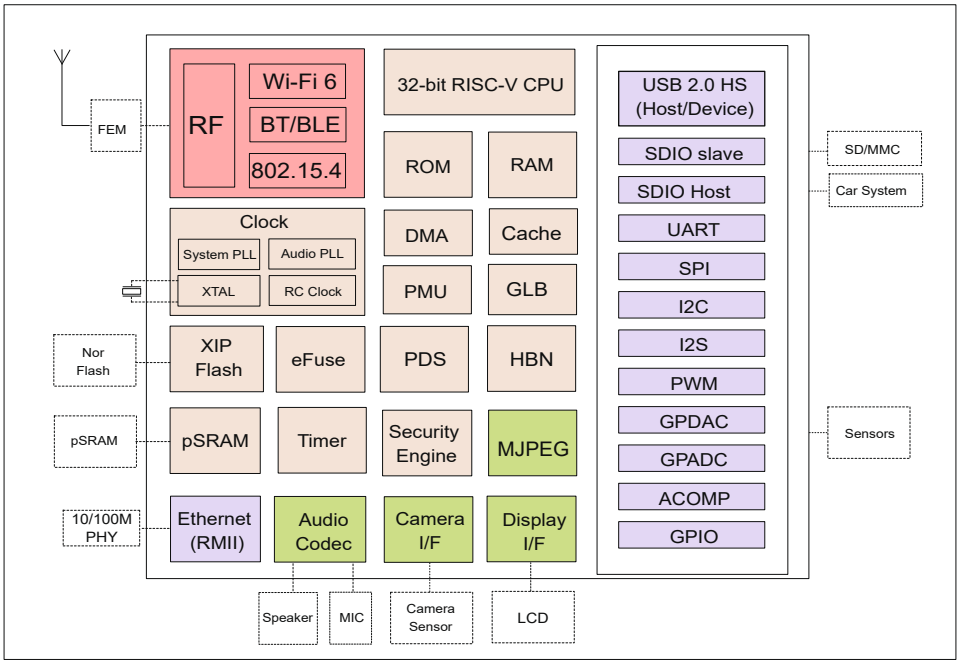

Fig. 1.1: Block Diagram

2 Functional Description

BL616/BL618 main functions described as follows:

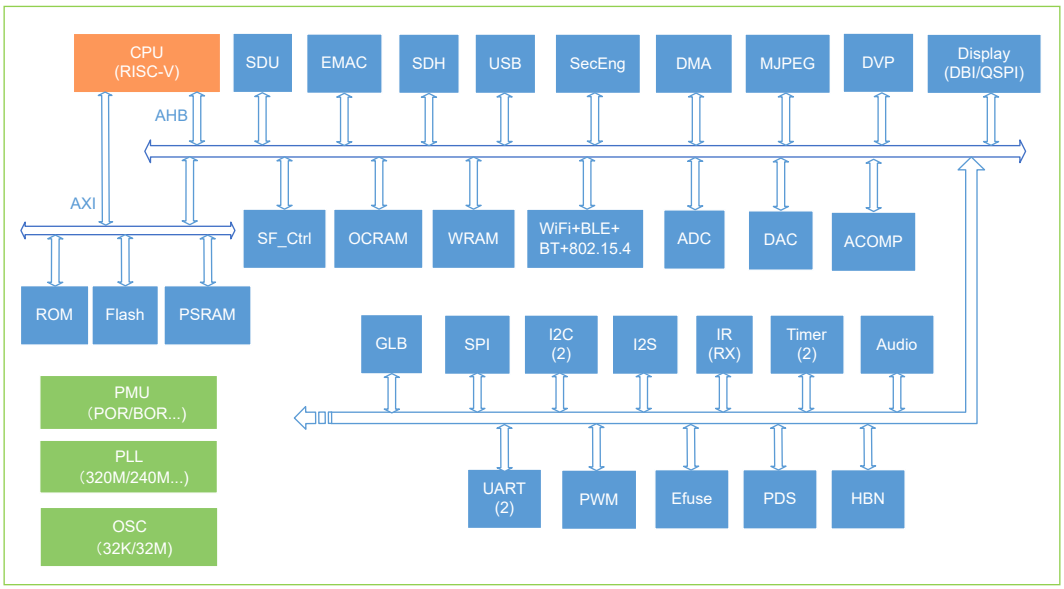

Fig. 2.1: System Architecture

2.1 CPU

BL616/BL618 has a built-in 32-bit RISC-V CPU, which adopts a 5-stage pipeline structure: fetch, decode, execute, memory access, write back, support RISC-V 32/16-bit mixed instruction set, including 64 external Interrupt source, there are 4 bits that can be used to configure the interrupt priority.

2.2 Cache

The cache of BL616/BL618 improves the performance of CPU accessing external memory, including 32K instruction cache and 16K data cache.

2.3 Memory

BL616/BL618 memory includes: on-chip zero-delay SRAM memory, read-only memory, write-once memory, Embedded flash (optional), embedded pSRAM (optional).

2.4 DMA

The DMA controller has 4 dedicated channels to manage data transfers between peripherals and memory to improve CPU/bus efficiency. DMA has four transfer types, memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral modes.

The DMA also supports the LLI (Linked List Item) feature, which consists of a series of linked lists that predefine multiple transfers, and then the hardware automatically completes all transfers based on the size and address of each LLI.

Peripherals supported by DMA include UART、I2C、SPI、Audio(Audio ADC and Audio DAC)、GPIO、I2S、DBI、GPADC、GPDAC.

2.5 Memory Map

Table 2.1: Memory address map

Module	Size	Base Address	
		Cache	Non-cache
OCRAM	320KB	0x62FC0000	0x22FC0000
WRAM	160KB	0x63010000	0x23010000

OCRAM and WRAM can be accessed either through the AHB bus or through AXI. When the CPU uses the 0x62FC0000 address to access the OCRAM, it will go through the internal cache and access the OCRAM through AXI to AHB. When the CPU uses the 0x22FC0000 address to access the OCRAM, it will directly access the OCRAM through the AHB bus.

Table 2.2: Memory Map

Module	Target	Base Address	Size	Description
FLASH	Flash	0xA0000000	128MB	Application address space

Table 2.2: Memory Map (continued)

Module	Target	Base Address	Size	Description
PSRAM	pSRAM	0xA8000000	128MB	pSRAM memory address space (optional, depends on the specific chip model)
RAM	HBN RAM	0x20010000	4KB	HBN RAM,mainly used for data saving in ultra-low power mode
Peripheral	USB	0x20072000	4KB	USB High Speed OTG Control Register
	EMAC	0x20070000	4KB	EMAC Control Register
	SDH	0x20060000	4KB	SDH Control Register
	MJPEG	0x20059000	4KB	MJPEG Control Register
	DVP	0x20057000	4KB	DVP camera interface Control Register
	Efuse	0x20056000	4KB	Efuse storage Control Register
	AUDIO PWM	0x20055000	4KB	Audio PWM Control Register
	PSRAM_Ctrl	0x20052000	4KB	PSRAM Control Register
	HBN	0x2000F000	4KB	Hibernate register
	PDS	0x2000E000	4KB	Power-down sleep register
	SDU	0x2000D000	4KB	SDU Control Register
	DMA	0x2000C000	4KB	DMA Control Register
	SF_Ctrl	0x2000B000	4KB	Serial Flash Control Register
	Audio ADC	0x2000AC00	256B	Audio ADC Control Register
	I2S	0x2000AB00	256B	I2S Control Register
	I2C1	0x2000A900	256B	I2C1 Control Register
	Display	0x2000A800	256B	Display Control Register
	IRR	0x2000A600	256B	IR Receiver Control Register
	TIMER	0x2000A500	256B	TIMER Control Register
	PWM	0x2000A400	256B	PWM Control Register
	I2C0	0x2000A300	256B	I2C0 Control Register
	SPI	0x2000A200	256B	SPI Control Register
	UART1	0x2000A100	256B	UART1 Control Register
	UART0	0x2000A000	256B	UART0 Control Register
	TZ	0x20005000	4KB	TrustZone Control Register
	SEC_ENG	0x20004000	4KB	Security Engine Control Register
	GPIP	0x20002000	1KB	General Purpose DAC/ADC/ACOMP Interface Control Register
	GLB	0x20000000	4KB	Global control register
ROM	ROM	0x90000000	128KB	Bootrom address space

2.6 Interrupt

BL616/BL618 supports internal RTC clock wake-up and external interrupt wake-up to realize low-power sleep wake-up function.

The CPU interrupt controller supports a total of 64 maskable interrupt trigger sources including UART interrupt, I2C interrupt, SPI interrupt, timer interrupt, DMA interrupt, etc.

All I/O pins can be configured as external interrupt input mode, the external interrupt supports nine trigger types: synchronous high/low level trigger, synchronous rising/falling edge trigger, asynchronous high/low level trigger, asynchronous rising edge /Falling edge trigger and synchronous double edge trigger.

2.7 Boot

BL616/BL618 supports multiple boot options: UART,USB,SDU and Flash.

Table 2.3: Boot mode

Boot pin	Level	Description
GPIO2	1	Boot from UART(GPIO21/22)/USB/SDU, this mode is mainly used for flash programming or downloading image to RAM for execution (wireless transparent transmission scenario)
	0	Launch application image from Flash

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into running, idle, sleep, hibernation and power off modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, PLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc.

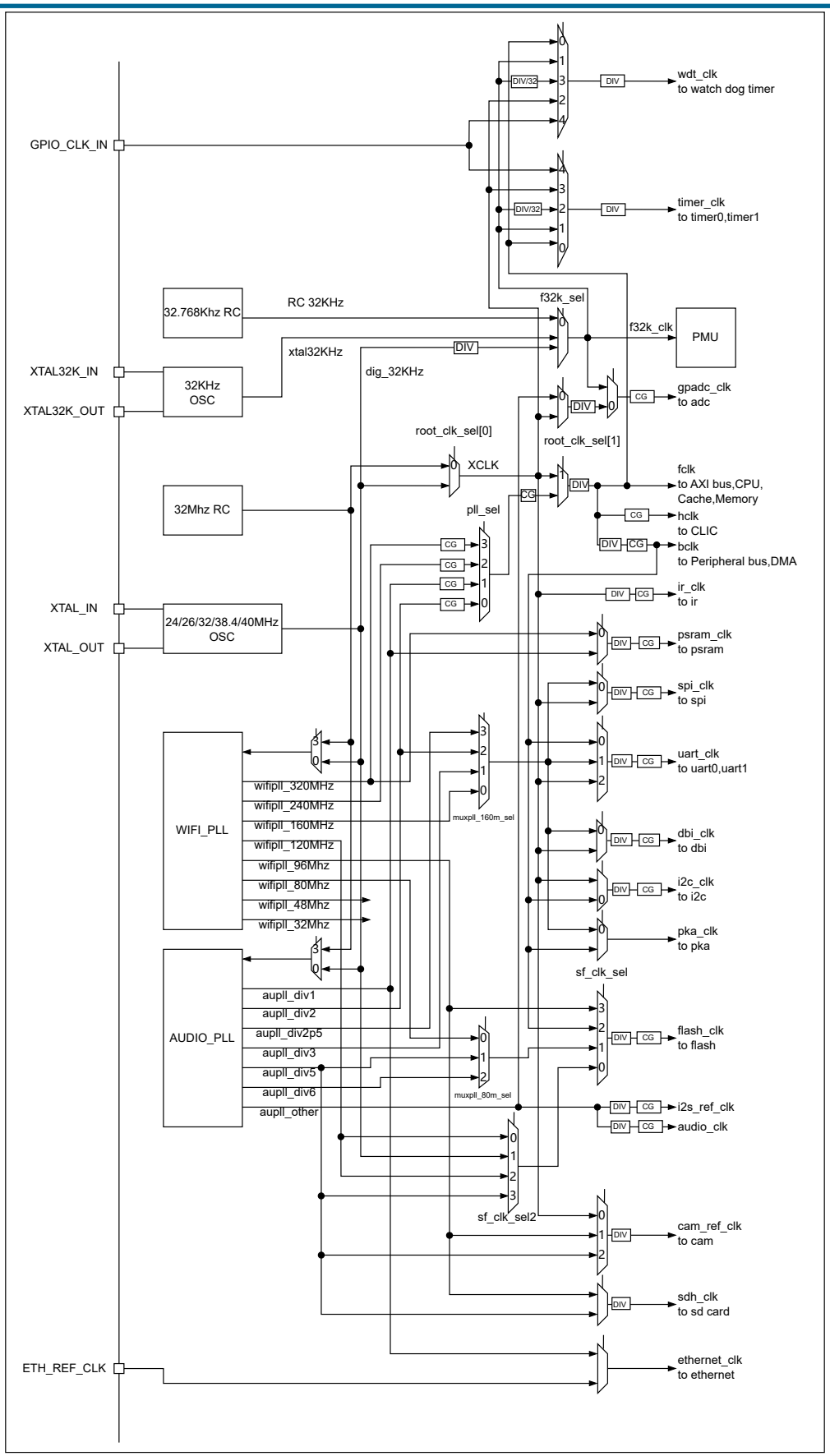

Fig. 2.2: Clock Architecture

2.10 Peripheral

Peripherals include GPIO, UART, SPI, I2C, PWM, Timer, IR(RX), Display(DBI/QSPI), I2S, Audio(Audio ADC+Audio DAC), SDU, DVP, MJPEG, SD/MMC(SDH), Ethernet MAC, GPDAC, GPADC, ACOMP, USB2.0.

2.10.1 GPIO

BL616 can have up to 19 GPIOs, BL618 can have up to 35 GPIOs, with the following features:

- Each GPIO can be used as general-purpose input and output function, pull-up/pull-down/float can be configured by software
- Each GPIO supports interrupt function, the interrupt supports synchronous high/low level trigger, synchronous rising/falling edge trigger, asynchronous high/low level trigger, asynchronous rising/falling edge trigger and synchronous double edge trigger
- Each GPIO can be set to high-impedance state for low-power modes

2.10.2 UART

The chip has two built-in universal asynchronous serial transceivers (UART0/1) with the following features:

- Supports CTS and RTS flow control in hardware
- Support LIN master/slave function
- Configurable data bits, stop bits and parity bits
- Supports automatic baud rate detection for common/fixed characters
- The working clock can be selected as FCLK, XCLK or 160MHz, the maximum baud rate supports 10Mbps
- TX and RX have independent FIFO, FIFO depth is 32 bytes, support DMA function

2.10.3 SPI

The chip has a built-in SPI, which can be configured as master mode or slave mode. The SPI module clock is XCLK or 160MHz, and has the following characteristics:

- In master mode, clock frequency up to 80 MHz
- In slave mode, the maximum allowed master clock frequency is 80 MHz
- The bit width of each frame can be configured as 8-bit / 16-bit / 24-bit / 32-bit
- Adaptive FIFO depth change characteristics, suitable for high-performance scene applications
  - When the bit width is 32 bits, the depth of the FIFO is 8
  - When the bit width is 24 bits, the depth of the FIFO is 8

  - When the bit width is 16 bits, the depth of the FIFO is 16
  - When the bit width is 8 bits, the depth of the FIFO is 32
- Support DMA transfer mode

2.10.4 I2C

The chip has two built-in I2C interfaces with the following features:

- Supports multi-master mode and arbitration function
- The working clock can be selected as BCLK or XCLK
- With device address register, register address register, register address length can be set to 1 byte/ 2 bytes/ 3 bytes/ 4 bytes
- I2C has independent transceiver FIFO, FIFO depth is 2 word
- Support DMA function

2.10.5 EMAC

The EMAC module is a 10/100Mbps Ethernet Media Access Controller (EMAC) compatible with IEEE 802.3, with the following features:

- Compatible with the MAC layer defined by IEEE 802.3
- PHY supporting MII/RMII interface defined by IEEE 802.3
- Interacts with PHY through MDIO interface
- Supports 10 Mbps and 100 Mbps Ethernet
- Supports half-duplex and full-duplex
- Supports automatic flow control and control frame generation in the full-duplex mode
- Supports collision detection and retransmission in the half-duplex mode
- Supports the generation and verification of CRC
- Generates and removes data frame preamble
- Supports automatic extension of short data frames when sending
- Detects too long/short data frames (length limit)
- Transmits long data frames (> standard Ethernet frame length)
- Automatically discards data packets with over-limit retransmission times or too small frame gap
- Broadcast packet filtering

- Internal RAM for storing up to 128 BDs
- Splits and configures a data packet to multiple consecutive Bds when sending
- Various event flags sent or received
- Generates a corresponding interrupt when an event occurs

The EMAC timing diagram is shown below:

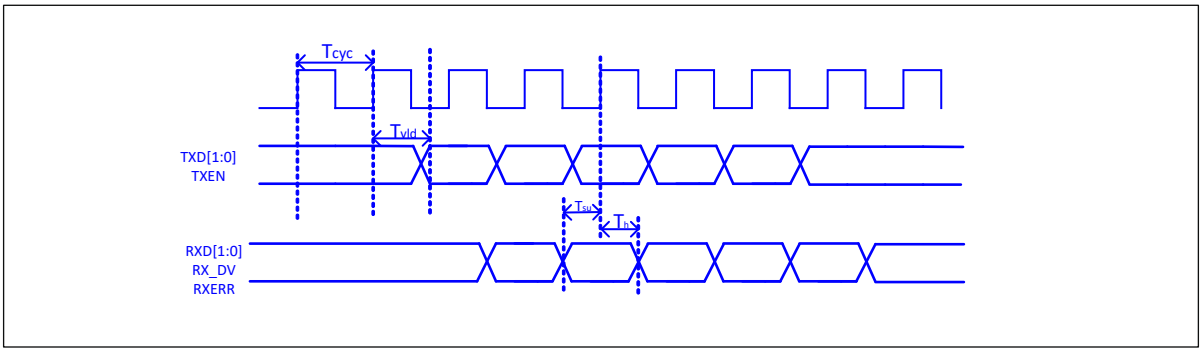

Fig. 2.3: EMAC Timing Diagram

Table 2.4: Timing conditions for using RX Clock

Set the corresponding bit of register eth_cfg0:cfg_inv_eth_rx_clk = 1 , cfg_inv_eth_tx_clk = 0 , cfg_sel_eth_ref_clk_o = 0						
Timing parameters(1.8V, Load = 20PF)		Min.	Typ	Max.	Unit	Note
T_{cyc}	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T_{vld}	Output Valid Delay	6.98	-	15.63	ns	TXD/TX_EN
T_{su}	Input Setup Time	11.64	-	-	ns	RXD/RX_DV/RXERR
T_h	Input Hold Time	0	-	-	ns	RXD/RX_DV/RXERR

Table 2.5: Timing conditions without using RX Clock

Set the corresponding bit of register eth_cfg0:cfg_inv_eth_rx_clk = 0 , cfg_inv_eth_tx_clk = 0 , cfg_sel_eth_ref_clk_o = 0						
Timing parameters(1.8V, Load = 20PF)		Min.	Typ	Max.	Unit	Note
T_{cyc}	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T_{vld}	Output Valid Delay	6.98	-	15.63	ns	TXD/TX_EN
T_{su}	Input Setup Time	3.5	-	-	ns	RXD/RX_DV/RXERR
T_h	Input Hold Time	2	-	-	ns	RXD/RX_DV/RXERR

2.10.6 I2S

The chip has a built-in I2S interface with the following features:

- Supports master mode as well as slave mode
- Support Left-justified/ Right-justified/ DSP and other data formats, the data width can be configured as 8/16/24/32 bits
- The working clock is Audio PLL
- Supports both four-channel and six-channel modes in addition to mono/dual-channel mode
- Supports playback of mono audio dubbing to binaural mode
- Support dynamic mute switching function
- I2S has independent transceiver FIFO, FIFO depth is 16 word
- Support DMA function

2.10.7 TIMER

The chip has two built-in 32-bit general-purpose timers and a watchdog timer with the following features:

- The clock source of the general timer can be selected from FCLK/32K/XTAL, and the clock source of the watchdog timer can be selected from FCLK/32K/XTAL
- 8-bit divider for each counter
- Each group of general-purpose timers includes three compare registers, supports compare interrupts, and supports FreeRun mode and PreLoad mode in counting mode
- 16-bit watchdog timer, supports two watchdog overflow modes: interrupt or reset

2.10.8 PWM

The chip has a built-in group of PWM signals, each group contains 4-channel PWM signal output, and each channel can be set to 2-channel complementary PWM, with the following characteristics:

- Three clock sources BCLK/XCLK/32K to choose from, with 16-bit clock divider
- Each group of PWM can be independently set to a different period
- Each channel PWM has dual threshold settings, which can set different duty cycles and phases to increase pulse elasticity
- Each channel PWM has independent dead time setting
- Each PWM output pin can be set to a different active level
- Each PWM has an independent connection switch to select whether to connect to the internal counter, and to set

the default output level when not connected

- Brake signal can put the PWM output level into a preset state
- Up to 11 trigger sources that can be used to trigger ADC conversions
- Supports multiple interrupt types: counter overflow interrupt, threshold value comparison interrupt, cycle count interrupt

2.10.9 IR(IR-remote)

The chip has a built-in infrared remote control with the following features:

- Supports receiving data with fixed protocols NEC, RC-5, and receiving data in any format with pulse width counting
- The clock source is XCLK, the maximum operating frequency is 40MHz
- Receive supports up to 64-bit data bits
- Receive FIFO depth of 128 bytes
- Support receive end interrupt

2.10.10 Audio ADC

- The chip has an integrated 1-channel audio ADC (not to be used simultaneously with the high precision ADC) with the following features:
  - Sampling rate:8k~96k
  - Signal-to-noise ratio (A-W): 96dB @ 6dB gain, 48K sampling rate
  - Harmonic distortion + noise: -90dB @ 6dB gain, 48K sample rate
  - Analogue preamp gain: 6 to 42 dB, 3dB steps
  - Analogue fully differential input or single-ended input
- Adjustable high-pass filter and digital volume control
- PDM interface support (1 way DMIC supported)
- Input signal multiplexing GPIO
- Transmit FIFO width of 32-bit, depth of 8
- Support for DMA transfer mode

2.10.11 Audio DAC

- Chip with integrated 1-channel audio DAC with the following features.
  - Sampling rate:8k~48k
  - Signal to noise ratio (A-W): 95dB @ 48K sample rate
  - Harmonic distortion + noise: -80dB @ 48K sample rate
- Adjustable digital volume control
- Supports differential complementary outputs
- Output signal multiplexing GPIO
- Transmit FIFO width of 32-bit, depth of 16
- Support for DMA transfer mode

2.10.12 GPADC

The chip has a built-in 12bits successive approximation analog-to-digital converter (ADC) with the following features.

- The maximum sampling rate of single-channel continuous conversion mode can reach 2M, and the maximum sampling rate of other conversion modes is 500K
- Supports 12 external analog channels
- Support single-channel single conversion, single-channel continuous conversion, multi-channel single conversion, multi-channel continuous conversion
- Supports 2.0V, 3.2V selectable internal reference voltages and 12/14/16bits (via oversampling) left-aligned conversion results
- 32-byte deep FIFO, multiple interrupt support, DMA support
- ADC can be used to measure supply voltages in addition to common analog signal measurements
- Can be used for temperature detection by measuring internal/external diode voltages

2.10.13 High precision ADC

- The chip has a built-in 1-channel high precision ADC (not to be used simultaneously with audio CODEC) with the following features.
  - Supports fully differential input, 4 channels
  - Effective resolution (ER): 19.5 bit
  - Programmable gain amplifier: 6dB to 42dB (2 to 128x), 3dB steps

  - Programmable data rates: 20SPS, 100SPS, 200SPS, 400SPS, 1000SPS, 2000SPS
  - Supports high accuracy/low latency dual set digital filters
  - Supports 50Hz/60Hz simultaneous frequency suppression
  - Supports software global chopping, ER=20.7bit, below 1uV detuning voltage
- Multiplexed GPIO input signals
- Transmit FIFO width of 32-bit, depth of 8
- Supports polling, interrupt and DMA transfer modes

3 Pin Definition

BL616 40-pin package includes 15 fixed power ports, 6 fixed analog ports, and up to 19 configurable GPIO ports.

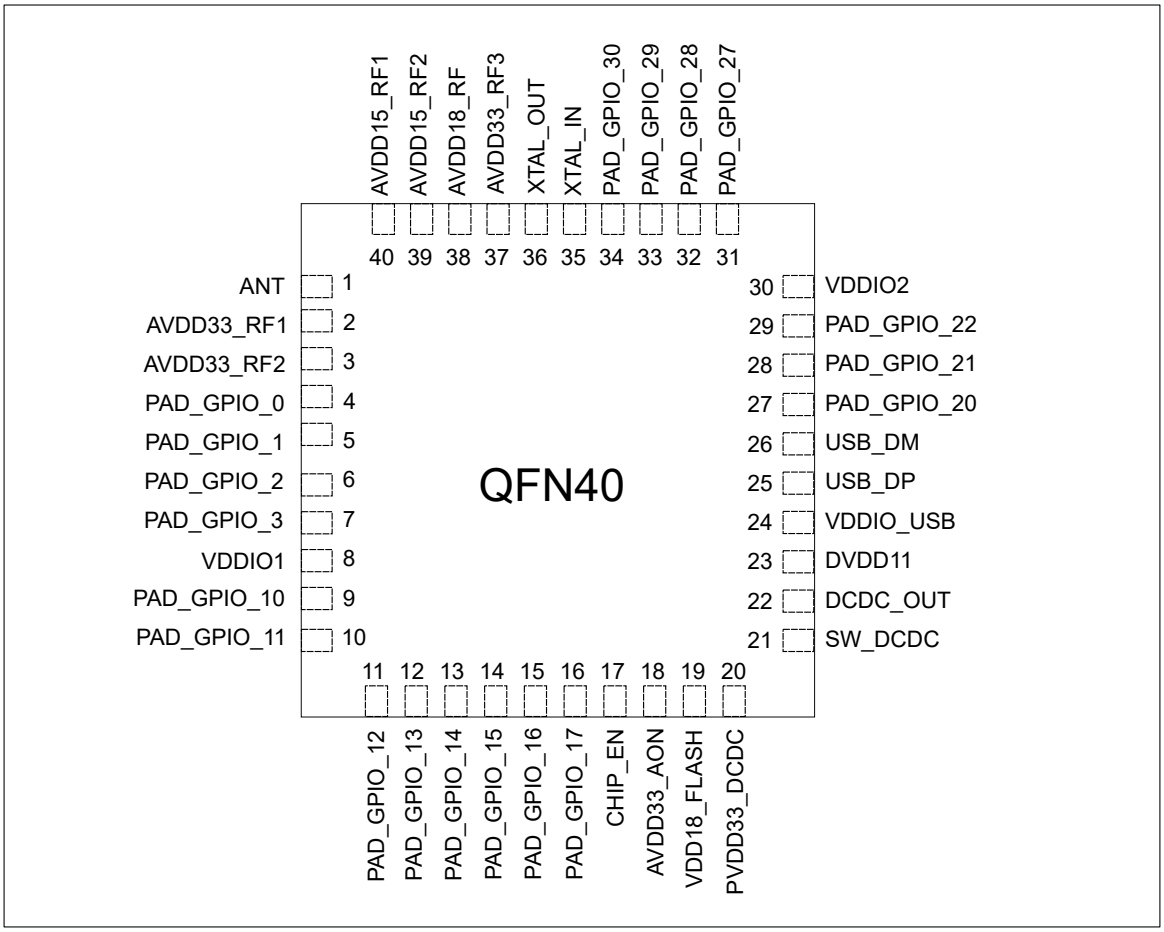

Fig. 3.1: BL616 pin layout

BL618 56-pin package includes 15 fixed power ports, 6 fixed analog ports, and up to 35 configurable GPIO ports.

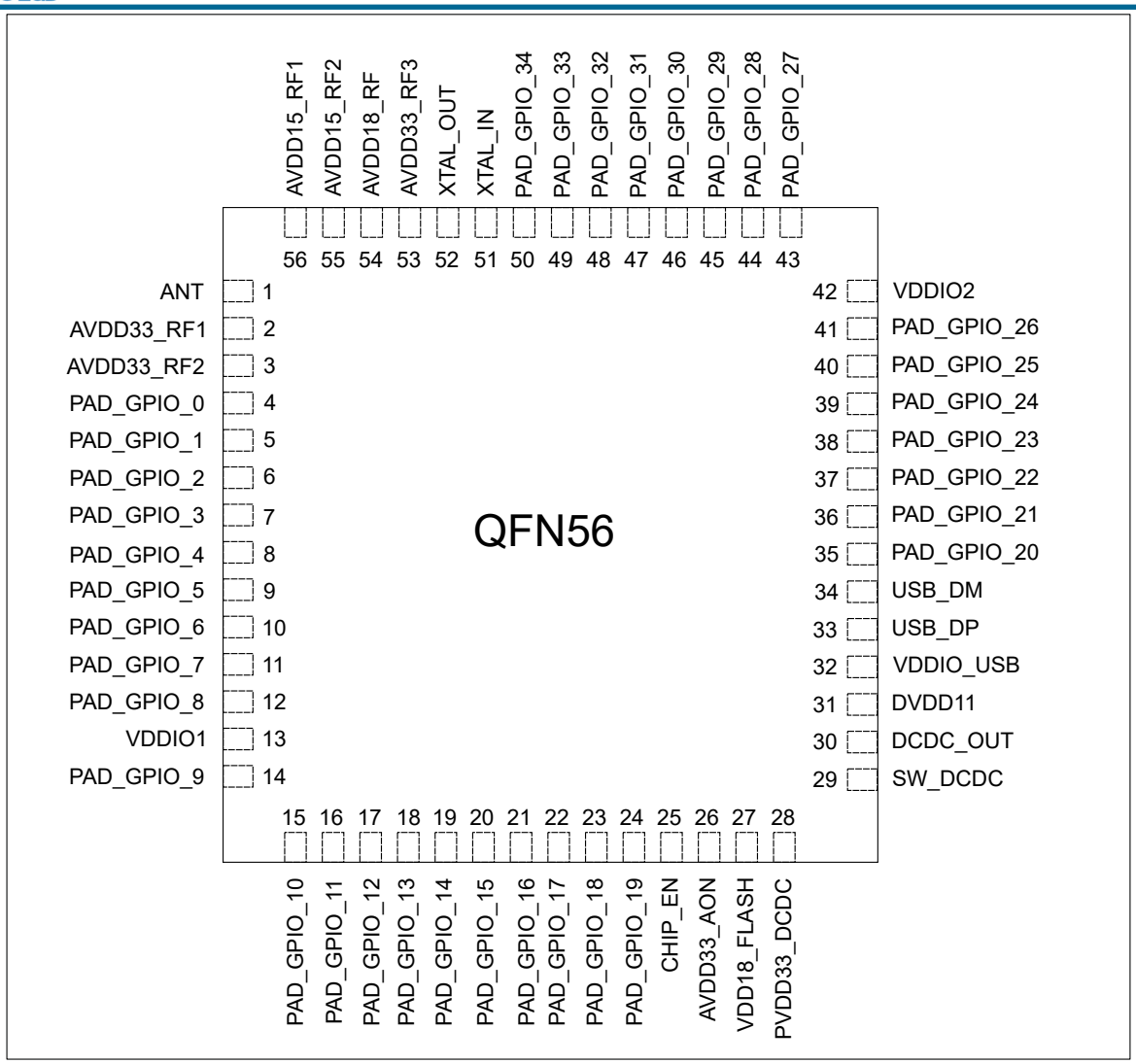

Fig. 3.2: BL618 pin layout

Table 3.1: Pin definition

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
1	1	AVDD15_RF1	Ana-log	ANT	-	-	ANT	RF signal pin
2	2	-	Power	AVDD33_RF1	-	-	AVDD33_RF1	RF transmitter power supply, 3.3V
3	3	-	Power	AVDD33_RF2	-	-	AVDD33_RF2	RF transmitter power supply, 3.3V

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
4	4	VDDIO_1	DI/DO	PAD_GPIO_0	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_VSYNC	CAM1_VSYNC
					10	-	ADC_CH9	ADC_CH9
					11	-	SWGPIO0	SWGPIO0
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
5	5	VDDIO_1	DI/DO	PAD_GPIO_1	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_HSYNC	CAM1_HSYNC
					10	-	ADC_CH8	ADC_CH8
					11	-	SWGPIO1	SWGPIO1
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
6	6	VDDIO_1	DI/DO	PAD_GPIO_2	0	-	-	
					1	-	SPI_MISO [1]	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH2	ADC_CH2
					11	-	SWGPIO2	SWGPIO2
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
7	7	VDDIO_1	DI/DO	PAD_GPIO_3	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_DAT0 [2]	CAM1_DAT0
					10	-	ADC_CH3	ADC_CH3
					11	-	SWGPIO3	SWGPIO3
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	8	VDDIO_1	DI/DO	PAD_GPIO_4	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	SF2_CS	SF2_CS
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO4	SWGPIO4
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					22	-	DBI_TypeB_WRn	DBI_TypeB_WRn
					23	-	DBI_TypeC_SCL	DBI_TypeC_SCL
					24	-	DISP_QSPI_SCL	DISP_QSPI_SCL
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
-	9	VDDIO_1	DI/DO	PAD_GPIO_5	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	SF2_D1	SF2_D1
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO5	SWGPIO5
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					22	-	DBI_TypeB_CSn	DBI_TypeB_CSn
					23	-	DBI_TypeC_CSn	DBI_TypeC_CSn
					24	-	DISP_QSPI_CSn	DISP_QSPI_CSn
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	10	VDDIO_1	DI/DO	PAD_GPIO_6	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	SF2_D2	SF2_D2
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO6	SWGPIO6
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					22	-	DBI_TypeB_RDn	DBI_TypeB_RDn
					23	-	DBI_TypeC_SDA0	DBI_TypeC_SDA0
					24	-	DISP_QSPI_SDA0	DISP_QSPI_SDA0
					25	-	-	
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
-	11	VDDIO_1	DI/DO	PAD_GPIO_7	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	SD2_D0	SD2_D0
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO7	SWGPIO7
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					22	-	DBI_TypeB_DCn	DBI_TypeB_DCn
					23	-	DBI_TypeC_DCn	DBI_TypeC_DCn
					24	-	DISP_QSPI_SDA1	DISP_QSPI_SDA1
					25	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	12	VDDIO_1	DI/DO	PAD_GPIO_8	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	SF2_CLK	SF2_CLK
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO8	SWGPIO8
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					22	-	DBI_TypeB_DB0	DBI_TypeB_DB0
					23	-	DBI_TypeC_SCL	DBI_TypeC_SCL
					24	-	DISP_QSPI_SDA2	DISP_QSPI_SDA2
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
8	13	-	Power	VDDIO1	-	-	VDDIO1	
-	14	VDDIO_1	DI/DO	PAD_GPIO_9	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	SF2_D3	SF2_D3
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO9	SWGPIO9
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					22	-	DBI_TypeB_DB1	DBI_TypeB_DB1
					23	-	DBI_TypeC_CSn	DBI_TypeC_CSn
					24	-	DISP_QSPI_SDA3	DISP_QSPI_SDA3
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
9	15	VDDIO_1	DI/DO	PAD_GPIO_10	0	-	SDH_DAT1	SDH_DAT1
					1	-	SPI_MISO	SPI_MISO
					2	-	SF2_D3	SF2_D3
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_DAT1	CAM1_DAT1
					10	-	ADC_CH7	ADC_CH7
					11	-	SWGPIO10	SWGPIO10
					12	-	SDIO_DAT2	SDIO_DAT2
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					22	-	DBI_TypeB_DB2	DBI_TypeB_DB2
					23	-	DBI_TypeC_SDA0	DBI_TypeC_SDA0
					24	-	DISP_QSPI_SCL	DISP_QSPI_SCL
					25	-	-	
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
10	16	VDDIO_1	DI/DO	PAD_GPIO_11	0		SDH_DAT0	SDH_DAT0
					1	-	SPI_MOSI	SPI_MOSI
					2	-	SF3_CLK	SF3_CLK
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_DAT2	CAM1_DAT2
					10	-	-	-
					11	-	SWGPIO11	SWGPIO11
					12	-	SDIO_DAT3	SDIO_DAT3
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					22	-	DBI_TypeB_DB3	DBI_TypeB_DB3
					23	-	DBI_TypeC_DCn	DBI_TypeC_DCn
					24	-	DISP_QSPI_CSn	DISP_QSPI_CSn
					25	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
11	17	VDDIO_1	DI/DO	PAD_GPIO_12	0		SDH_CLK	SDH_CLK
					1	-	SPI_SS	SPI_SS
					2	-	SF3_D0	SF3_D0
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_DAT3	CAM1_DAT3
					10	-	ADC_CH6	ADC_CH6
					11	-	SWGPIO12	SWGPIO12
					12	-	SDIO_CMD	SDIO_CMD
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					22	-	DBI_TypeB_DB4	DBI_TypeB_DB4
					23	-	DBI_TypeC_SCL	DBI_TypeC_SCL
					24	-	DISP_QSPI_SDA0	DISP_QSPI_SDA0
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
12	18	VDDIO_1	DI/DO	PAD_GPIO_13	0	-	SDH_CMD	SDH_CMD
					1	-	SPI_SCLK	SPI_SCLK
					2	-	SF3_D2	SF3_D2
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_CLK	CAM1_CLK
					10	-	ADC_CH5	ADC_CH5
					11	-	SWGPIO13	SWGPIO13
					12	-	SDIO_CLK	SDIO_CLK
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					22	-	DBI_TypeB_DB5	DBI_TypeB_DB5
					23	-	DBI_TypeC_CSn	DBI_TypeC_CSn
					24	-	DISP_QSPI_SDA1	DISP_QSPI_SDA1
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
13	19	VDDIO_1	DI/DO	PAD_GPIO_14	0		SDH_DAT3	SDH_DAT3
					1	-	SPI_MISO	SPI_MISO
					2	-	SF3_D1	SF3_D1
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_DAT4	CAM1_DAT4
					10	-	ADC_CH4	ADC_CH4
					11	-	SWGPIO14	SWGPIO14
					12	-	SDIO_DAT0	SDIO_DAT0
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					22	-	DBI_TypeB_DB6	DBI_TypeB_DB6
					23	-	DBI_TypeC_SDA0	DBI_TypeC_SDA0
					24	-	DISP_QSPI_SDA2	DISP_QSPI_SDA2
					25	-	AUPWM_P	AUPWM_P
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
14	20	VDDIO_1	DI/DO	PAD_GPIO_15	0		SDH_DAT2	SDH_DAT2
					1	-	SPI_MOSI	SPI_MOSI
					2	-	SF3_CS	SF3_CS
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	I2C1_SDA	I2C1_SDA
					10	-	-	-
					11	-	SWGPIO15	SWGPIO15
					12	-	SDIO_DAT1	SDIO_DAT1
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					22	-	DBI_TypeB_DB7	DBI_TypeB_DB7
					23	-	DBI_TypeC_DCn	DBI_TypeC_DCn
					24	-	DISP_QSPI_SDA3	DISP_QSPI_SDA3
					25	-	AUPWM_N	AUPWM_N
					26	-	M0_JTAG_TDI	M0_JTAG_TDI

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
15	21	AVDD33_AON	DI/DO	PAD_GPIO_16	-	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_DAT6	CAM1_DAT6
					10	-	-	-
					11	-	SWGPIO16	SWGPIO16
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
16	22	AVDD33_AON	DI/DO	PAD_GPIO_17	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM1_DAT7	CAM1_DAT7
					10	-	-	-
					11	-	SWGPIO17	SWGPIO17
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	23	AVDD33_AON	DI/DO	PAD_GPIO_18	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO18	SWGPIO18
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
-	24	AVDD33_AON	DI/DO	PAD_GPIO_19	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH1	ADC_CH1
					11	-	SWGPIO19	SWGPIO19
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
17	25	AVDD33_AON	Ana-log	CHIP_EN			CHIP_EN	CHIP_EN
18	26	-	Power	AVDD33_AON	-	-	AVDD33_AON	
19	27	-	Power	VDD18_FLASH	-	-	VDD18_FLASH	

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
20	28	-	Power	PVDD33_DCDC	-	-	PVDD33_DCDC	
21	29	-	Power	SW_DCDC	-	-	SW_DCDC	
22	30	-	Power	DCDC_OUT	-	-	DCDC_OUT	
23	31	-	Power	DVDD11	-	-	DVDD11	
24	32	-	Power	VDDIO_USB	-	-	VDDIO_USB	
25	33	VDDIO_USB	DI/DO	USB_DP			USB_DP	
26	34	VDDIO_USB	DI/DO	USB_DM			USB_DM	
27	35	VDDIO_2	DI/DO	PAD_GPIO_20	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH0	ADC_CH0
					11	-	SWGPIO20	SWGPIO20
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
28	36	VDDIO_2	DI/DO	PAD_GPIO_21	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO21	SWGPIO21
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK
29	37	VDDIO_2	DI/DO	PAD_GPIO_22	0	-	-	-
					1	-	SPI_MISO	SPI MOSI
					2	-	-	
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO22	SWGPIO22
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUPWM_P	AUPWM_P
					26	-	M0_JTAG_TDO	M0_JTAG_TDO

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	38	VDDIO_2	DI/DO	PAD_GPIO_23	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO23	SWGPIO23
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUPWM_N	AUPWM_N
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
-	39	VDDIO_2	DI/DO	PAD_GPIO_24	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
					8	-	-	-
					9	-	CAM0_DAT0	CAM0_DAT0
					10	-	-	-
					11	-	SWGPIO24	SWGPIO24
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	40	VDDIO_2	DI/DO	PAD_GPIO_25	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_REF_CLK	RMII_REF_CLK
					9	-	CAM0_DAT1	CAM0_DAT1
					10	-	-	-
					11	-	SWGPIO25	SWGPIO25
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK
-	41	VDDIO_2	DI/DO	PAD_GPIO_26	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_TXD[0]	RMII_TXD[0]
					9	-	CAM0_DAT2	CAM0_DAT2
					10	-	-	-
					11	-	SWGPIO26	SWGPIO26
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
30	42	-	Power	VDDIO2	-	-	VDDIO2	

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
31	43	VDDIO_2	DI/DO	PAD_GPIO_27	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_TXD[1]	RMII_TXD[1]
					9	-	CAM0_DAT3	CAM0_DAT3
					10	-	ADC_CH10	ADC_CH10
					11	-	SWGPIO27	SWGPIO27
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUPWM_N	AUPWM_N
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
32	44	VDDIO_2	DI/DO	PAD_GPIO_28	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_RXD[0]	RMII_RXD[0]
					9	-	CAM0_HSYNC	CAM0_HSYNC
					10	-	-	-
					11	-	SWGPIO28	SWGPIO28
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUPWM_P	AUPWM_P
					26	-	M0_JTAG_TMS	M0_JTAG_TMS

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
33	45	VDDIO_2	DI/DO	PAD_GPIO_29	0	-	-	-
					1	-	SPI_SCLK	SPI SCLK
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_RXD[1]	RMII_RXD[1]
					9	-	CAM0_VSYNC	CAM0_VSYNC
					10	-	-	-
					11	-	SWGPIO29	SWGPIO29
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK
34	46	VDDIO_2	DI/DO	PAD_GPIO_30	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_RXERR	RMII_RXERR
					9	-	CAM0_CLK	CAM0_CLK
					10	-	-	-
					11	-	SWGPIO30	SWGPIO30
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	47	VDDIO_2	DI/DO	PAD_GPIO_31	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_TX_EN	RMII_TX_EN
					9	-	CAM0_DAT4	CAM0_DAT4
					10	-	-	-
					11	-	SWGPIO31	SWGPIO31
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
-	48	VDDIO_2	DI/DO	PAD_GPIO_32	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_RX_DV	RMII_RX_DV
					9	-	CAM0_DAT5	CAM0_DAT5
					10	-	-	-
					11	-	SWGPIO32	SWGPIO32
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	49	VDDIO_2	DI/DO	PAD_GPIO_33	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_MDC	RMII_MDC
					9	-	CAM0_DAT6	CAM0_DAT6
					10	-	-	-
					11	-	SWGPIO33	SWGPIO33
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0_JTAG_TCK
-	50	VDDIO_2	DI/DO	PAD_GPIO_34	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
					8	-	RMII_MDIO	RMII_MDIO
					9	-	CAM0_DAT7	CAM0_DAT7
					10	-	-	-
					11	-	SWGPIO34	SWGPIO34
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
35	51	AVDD33_RF3	Clock	XTAL_IN			XTAL_IN	
36	52	AVDD33_RF3	Clock	XTAL_OUT			XTAL_OUT	
37	53	-	Power	AVDD33_RF3	-	-	AVDD33_RF3	

Table 3.1: Pin definition(continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
38	54	-	Power	AVDD18_RF	-	-	AVDD18_RF	
39	55	-	Power	AVDD15_RF2	-	-	AVDD15_RF2	
40	56	-	Power	AVDD15_RF1	-	-	AVDD15_RF1	

1 This function defaults to SPI_MISO, which can be converted to SPI_MOSI through a register.

2 Only one of CAM0 and CAM1 can be selected.

4 Audio characteristic

Table 4.1: AUADC performance

At 25°C, VDDIO= 3.3 V, f_S= 48kHz, 16-bit audio data (unless otherwise noted)						
Parameter		Conditions	Min.	Typ	Max.	Unit
AUDIO ADC	Input signal full-scale level	differential input，6dB PGA gain		1.16		Vrms
		Single-ended input，6dB PGA gain		0.8		
	Input common-mode voltage	differential/Single-ended input		1.57		V
SNR	Signal-to-noise ratio, A-weighted	f_S= 48 kHz, 0 dB PGA gain, 1kHz full-scale sine-wave input		96		dB
DR	Dynamic range, A-weighted	f_S= 48 kHz, 0 dB PGA gain, 1kHz -60dB sine-wave input		95		
THD	Total harmonic distortion	f_S= 48 kHz, 0 dB PGA gain, 1kHz -5dB sine-wave input		-90		
Freq. Response(20Hz~16kHz)		-5dB sine-wave input		±0.13		
ADC programmable analogue amplifier gain range		Analogue gain resolution = 3dB	6		42	
ADC programmable digital gain range		Digital gain resolution = 0.5dB	-95.5		31.5	
Input resistance		Analogue gain 6dB~42dB	160K		480	kΩ

Table 4.2: AUDAC performance

At 25°C, VDDIO= 3.3 V, f_S= 48kHz, @AUDAC_P/N with RC filter(R=1KΩ , C=470pF) (unless otherwise noted)						
Parameter		Conditions	Min.	Typ	Max.	Unit
AUDIO DAC	Input signal full-scale level	Differential output，0 dB line-out gain		1.8		Vrms
SNR	Signal-to-noise ratio, A-Weighted	f_S= 48 kHz, 1kHz full-scale sine-wave output		95		dB

Table 4.2: AUDAC performance(continued)

At 25°C, VDDIO= 3.3 V, f_S= 48kHz, @AUDAC_P/N with RC filter(R=1KΩ , C=470pF) (unless otherwise noted)						
Parameter		Conditions	Min.	Typ	Max.	Unit
DR	Dynamic range, A-weighted	f_S= 48 kHz, 1kHz -60dB sine-wave output		95		
THD	Total harmonic distortion	f_S= 48 kHz, 1kHz -5dB sine-wave output		-80		
Noise Floor		Play 0data @ No A-weighted		26		Vrms
Freq. Response(20Hz~16kHz)		-5dB sine-wave input		±0.25		dB
programmable digital gain range		Digital gain resolution = 0.5dB	-95.5		31.5	

5 Electrical Specifications

5.1 Absolute Maximum Rating

Table 5.1: Absolute Maximum Rating

Pin Name	Min.	Max.	Unit
AVDD33_RF1, AVDD33_RF2, AVDD33_AON, PVDD33_DCDC, VDDIO_USB, AVDD33_RF3	-0.3	3.63	V
VDDIO1, VDDIO2	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-45	135	°C

5.2 Operating Condition

5.2.1 Power characteristics

Table 5.2: Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
AVDD33_RF1, AVDD33_RF2, AVDD33_AON, PVDD33_DCDC, VDDIO_USB, AVDD33_RF3	2.97	3.3	3.63	V
VDDIO1, VDDIO2	2.97/1.62	3.3/1.8	3.63/1.98	

5.2.2 IO DC characteristics

Test conditions:VDDIO = 3.3V, temperature = 25°C

Table 5.3: IO DC characteristics

Sym-bol	Description	GPIO num	Conditions	Min.	Typ	Max.	Unit
VOH	Output voltage high	GPIO 21-22, GPIO28-29	GPIO drive strength 0, source current = 12mA		0.9*VDDIO		V
			GPIO drive strength 1, source current = 36.1mA				
			GPIO drive strength 2, source current = 72.2mA				
			GPIO drive strength 3, source current = 96mA				
		GPIO 0-20, GPIO 23-27, GPIO 30-34	GPIO drive strength 0, source current = 9.7mA				
			GPIO drive strength 1, source current = 29.2mA				
			GPIO drive strength 2, source current = 58.5mA				
			GPIO drive strength 3, source current = 80mA				
VOL	Output voltage low	GPIO 21-22, GPIO28-29	GPIO drive strength 0, sink current = 11mA				V
			GPIO drive strength 1, sink current = 38.4mA				
			GPIO drive strength 2, sink current = 71.4mA				
			GPIO drive strength 3, sink current = 99mA				
		GPIO 0-20, GPIO 23-27, GPIO 30-34	GPIO drive strength 0, sink current = 11.4mA				
			GPIO drive strength 1, sink current = 34mA				
			GPIO drive strength 2, sink current = 68.5mA				
			GPIO drive strength 3, sink current = 91mA				
VIH	Input voltage high			0.7*VD-DIO			V
VIL	Input voltage low					0.3*VD-DIO	V

5.2.3 Power-on sequence

In order to ensure normal power-on startup, the power, reset and Bootstrap pins need to meet the corresponding timing requirements.

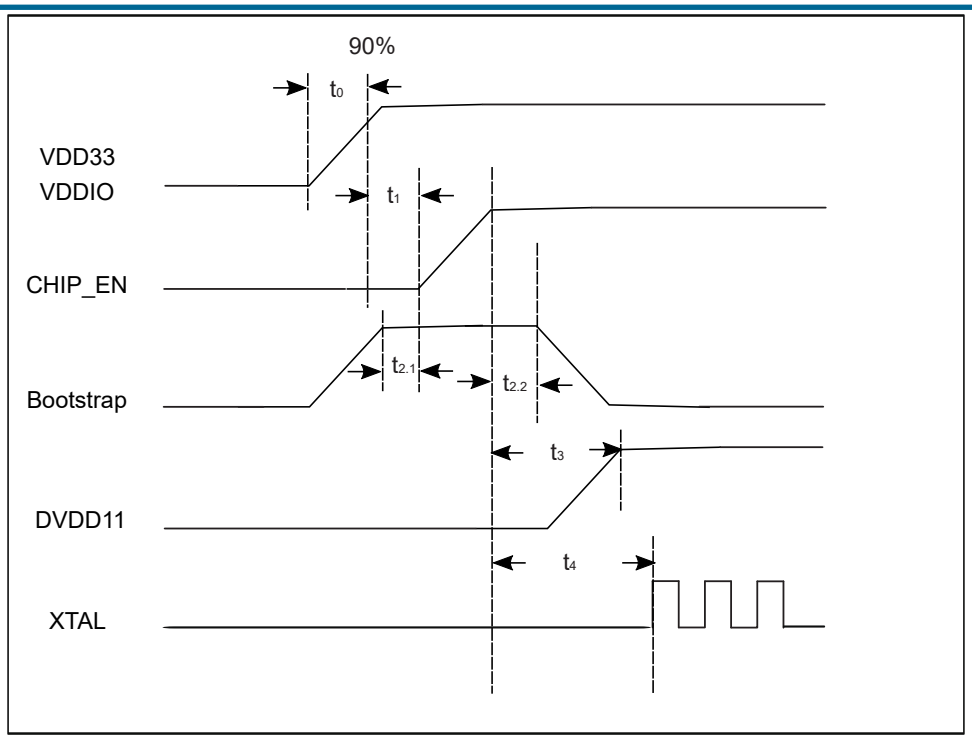

Fig. 5.1: Power-on sequence

Table 5.4: Power-on sequence parameters

Parame-ters	Description	Min.(ms)	Typ(ms)	Max.(ms)
t_0	The power supply voltage reaches 90% rise time			2
t_1	The delay between the completion of power up and CHIP_EN high	0.1		
$t_{2.1}$	Bootstrap pin [1] level setup time before CHIP_EN is pulled high	0		
$t_{2.2}$	The hold time of the Bootstrap pin level after CHIP_EN is pulled high	2		
t_3	The time between CHIP_EN is pulled high and DVDD11 output		2	
t_4	The time between CHIP_EN is pulled high and XTAL starting to oscillate		2	

[1] Bootstrap pin is GPIO2.

5.2.4 Temperature sensor characteristics

Table 5.5: Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	-40	105	°C
	Multi-Die SiP	-40	85	°C

5.2.5 General operating conditions

Table 5.6: General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
FCPU	CPU/TCM/Cache clock frequency		320		MHz
FBUS	System bus clock frequency		80		MHz

6 Product use

6.1 Moisture Sensitivity Level(MSL)

The moisture sensitivity level of the chip is: MSL3. After the vacuum package is opened, it needs to be used up within 168 hours (7 days) at ≤30°C/60%RH, otherwise it needs to be baked and put online.

For baking temperature and time, please refer to IPC/JEDECJ-STD-033B01.

Table 6.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

6.2 Electro-Static discharge（ESD）

- Human Body Model(HBM): 2000V
- Charged-Device Model(CDM): 500V

6.3 Reflow Profile

For details, please refer to IPC/JEDEC J-STD-020E.

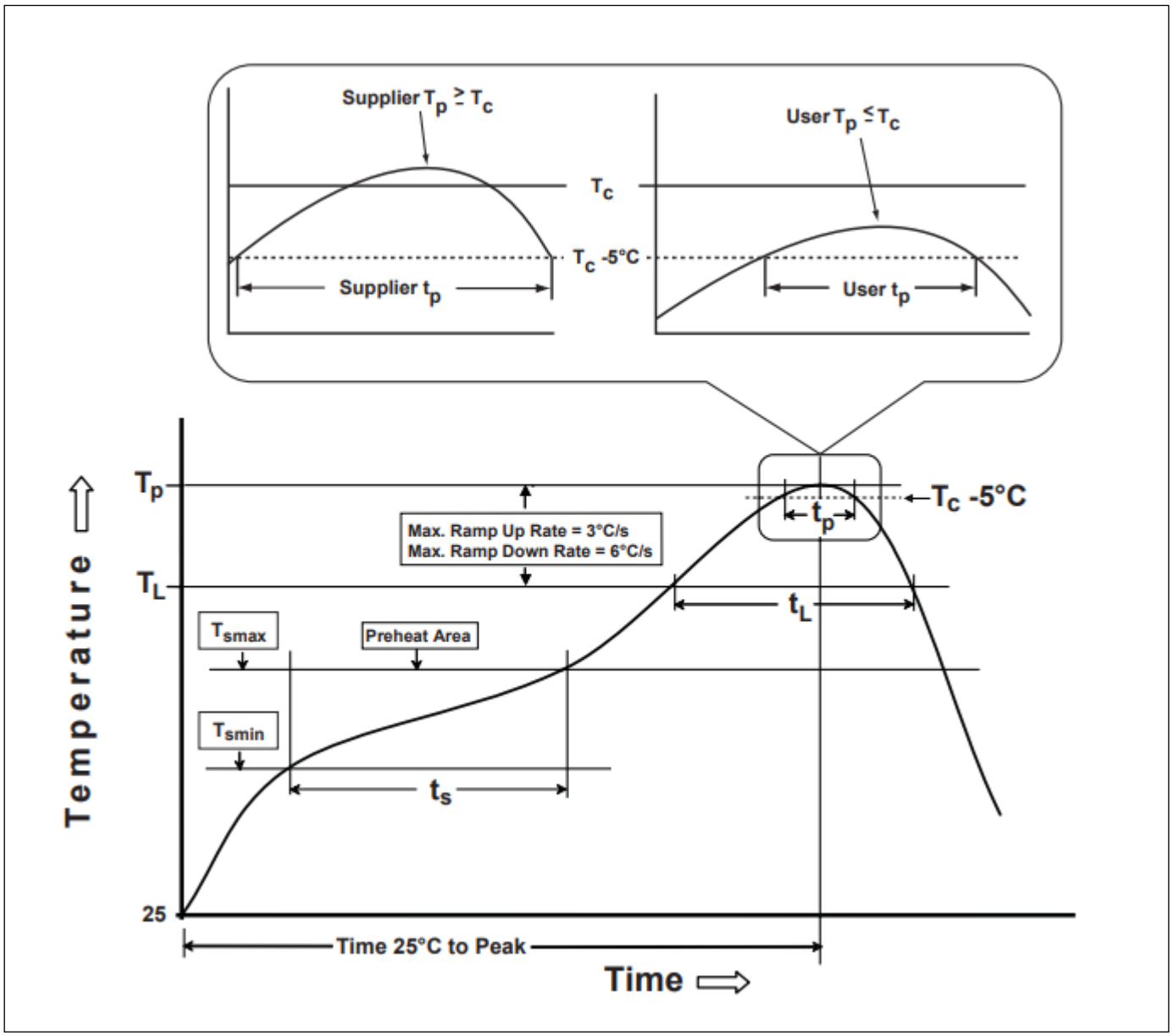

Fig. 6.1: Classification Profile (Not to scale)

Table 6.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	240 °C+0/-5 °C	250 °C+0/-5 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

7 Reference Design

8 Package Information(QFN40)

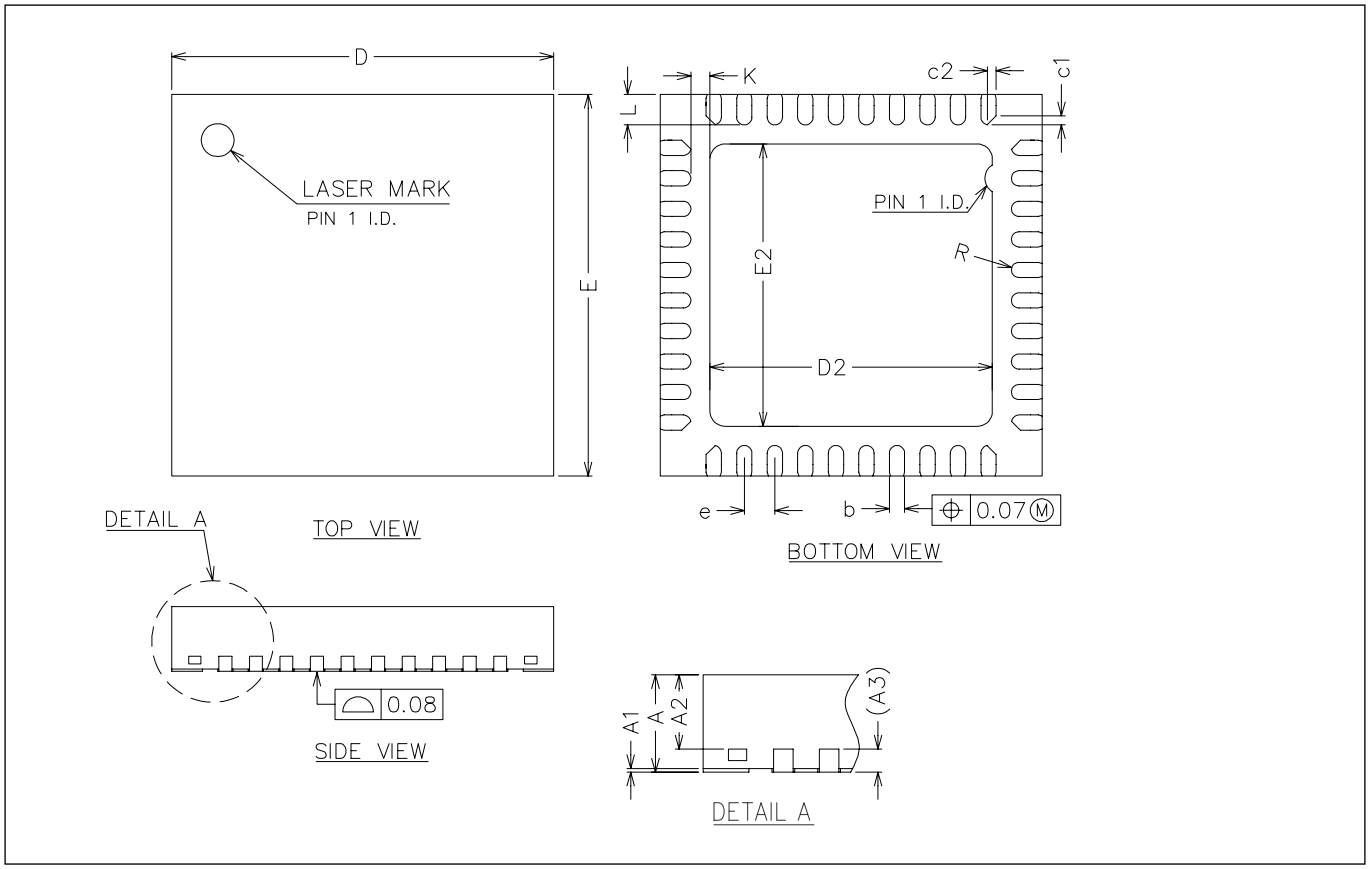

Fig. 8.1: QFN40 Package drawing

Table 8.1: QFN40 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90

Table 8.1: QFN40 Size Description(continued)

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.12	-
c2	-	0.12	-

9 Package Information(QFN56)

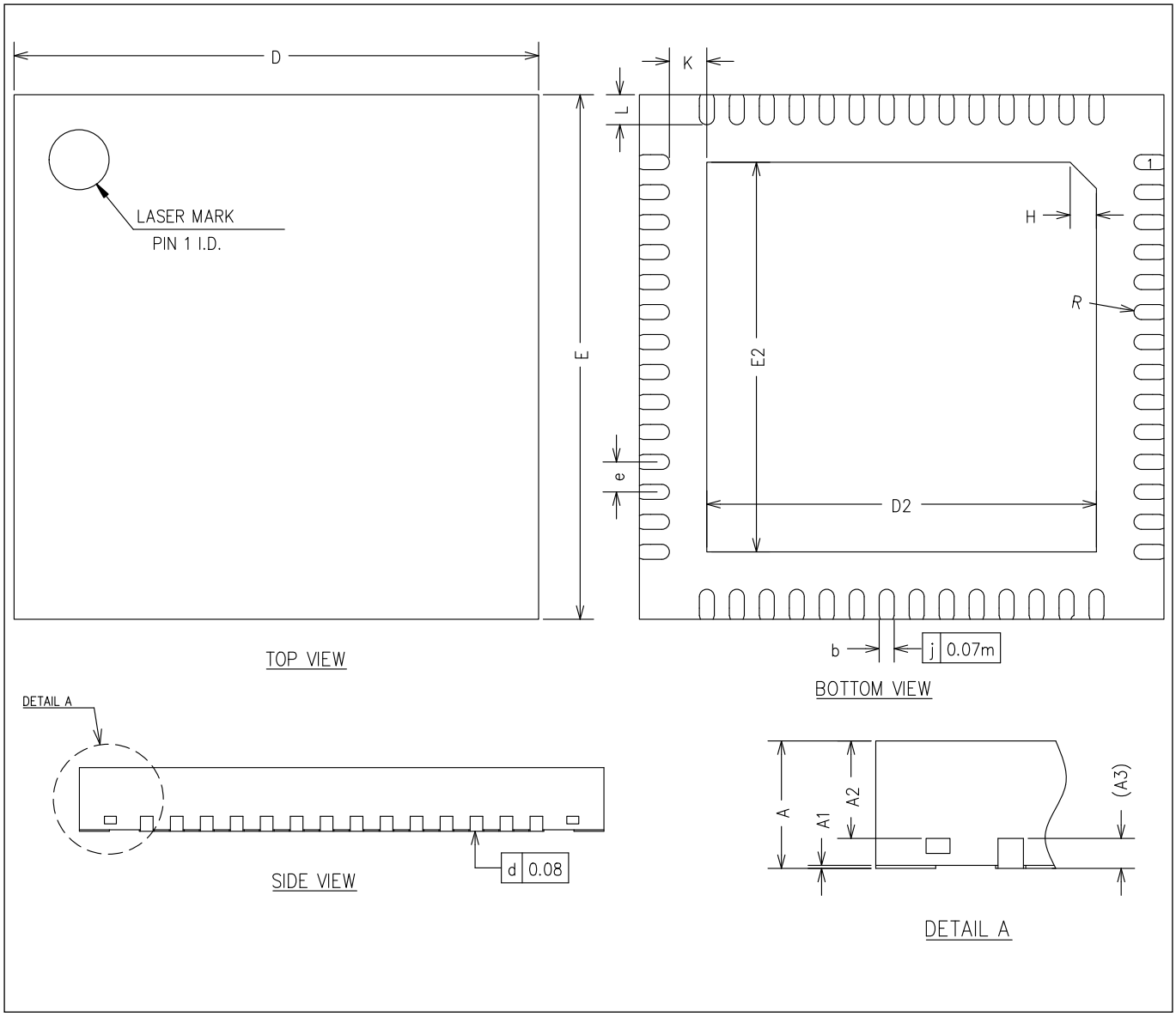

Fig. 9.1: QFN56 Package drawing

Table 9.1: QFN56 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 REF		
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
e	0.30	0.40	0.50
H	0.35 REF		
K	0.50 REF		
L	0.35	0.40	0.45
R	0.09	-	-

10 Top Marking Definition

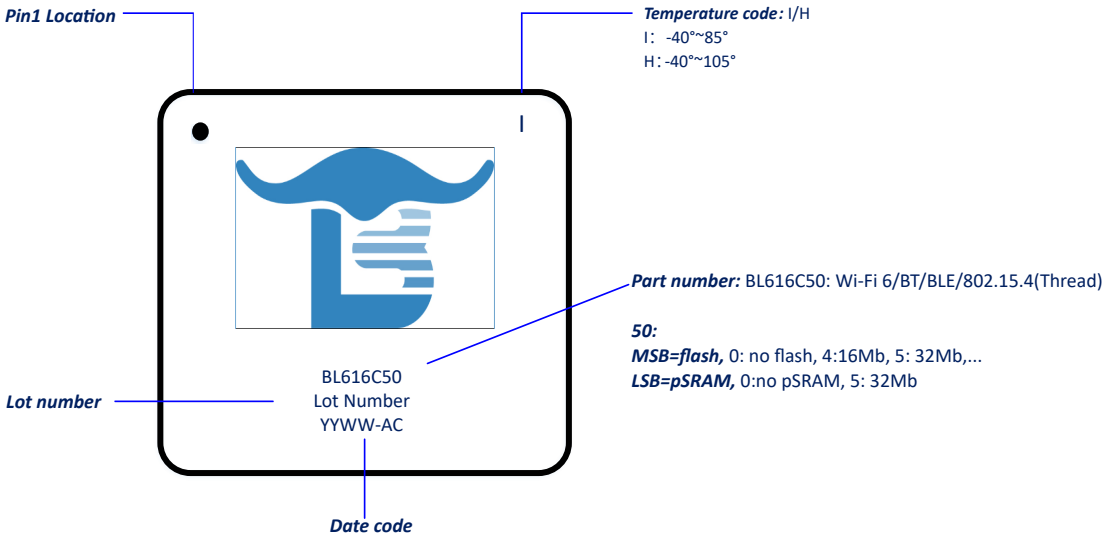

Fig. 10.1: Top Marking Definition

11 Ordering Information

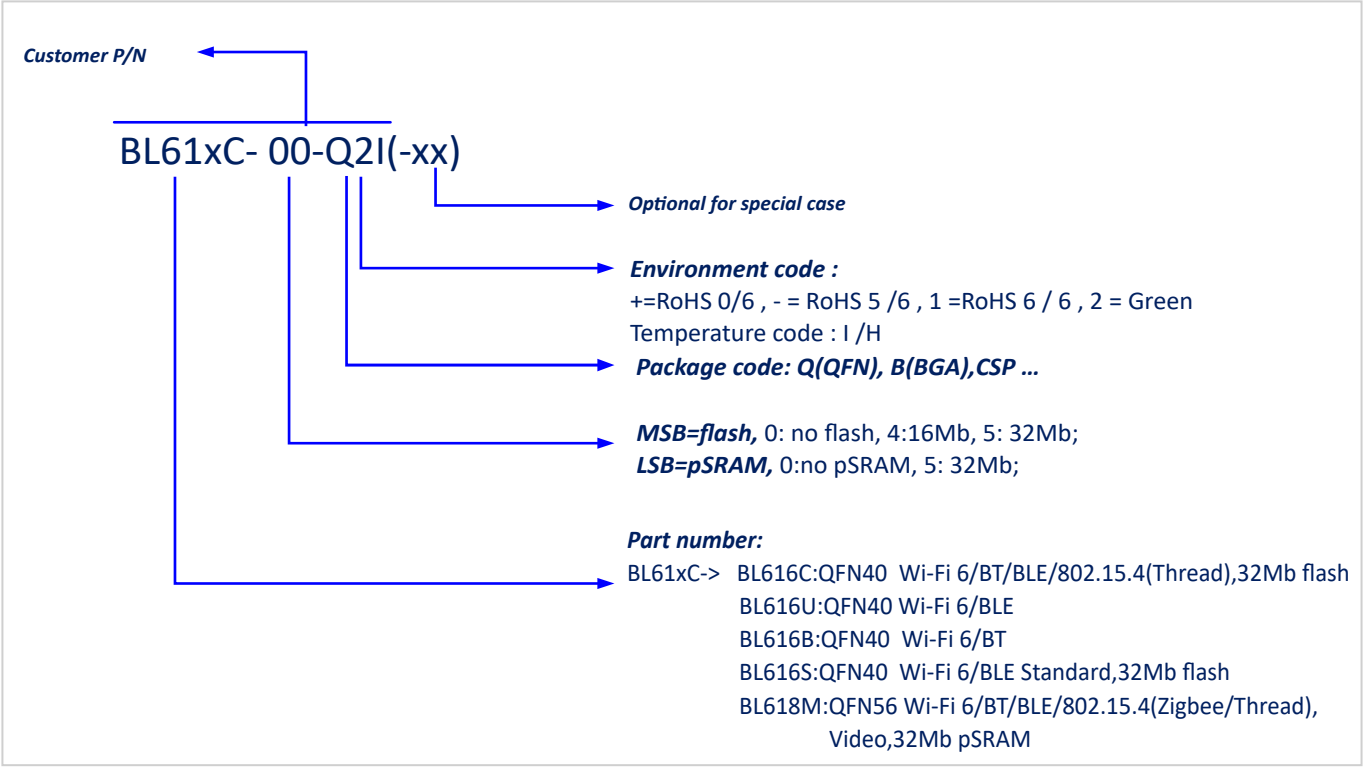

Fig. 11.1: Part Number

Table 11.1: Part Order Options

Customer P/N	Type	Package Size(mm)	MOQ	Description
BL616C-50-Q2I	QFN40	5x5x0.85, Pitch 0.4	6K	Wi-Fi 6/BT/BLE/802.15.4(Thread), 32Mb flash
BL616S-50-Q2I	QFN40	5x5x0.85, Pitch 0.4	6K	Wi-Fi 6/BLE Standard, 32Mb flash
BL618M-05-Q2I	QFN56	7x7x0.85, Pitch 0.4	3K	Wi-Fi 6/BT/BLE/802.15.4(Zigbee/Thread), Video, 32Mb pSRAM

12 Revision history

Table 12.1: Document revision history

Date	Revision	Changes
2022/3/10	0.9	Initial release
2022/5/12	0.92	Add package information and mark definition
2022/5/18	0.93	Add EMAC timing description
2022/6/7	0.94	Add electrical characteristics and ordering information
2022/8/9	0.95	Add audio performance
2022/8/18	0.96	Add spi and uart function descriptions, and add temperature descriptions
2022/8/26	1.0	Modify ordering information
2023/2/7	1.1	Ordering information add BL616S-50-Q2I description
2023/3/14	1.2	Add audio module description
2023/3/21	1.3	Delete GPIO21/22/28/29 analog function
2023/3/27	1.4	add GPADC module description
2023/5/10	1.5	Update Clock Tree Diagram